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Integration of Bus Specific Clock Gating and Power Gating

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Abstract: In integrated circuits a gargantuan portion of chip power is mostly consumed by clocking systems which comprises of flip-flops, latches and clock distribution networks. The two most widely used techniques for the reduction of dynamic and leakage power are clock gating (CG) and power gating (PG). The two techniques CG and PG are coupled in such a way that the clock enable signal is generated by CG used as sleep signal to drive the power gated cells for the reduction of leakage power. So here we first introduced bus specific clock gating (BSCG) technique which is traditional XOR based CG and it reduces the dynamic power, then the power gating (PG) technique is used for power gated cells for reduction of leakage power. All circuitsare simulated in CadenceVirtuso Analog Design Environment using GPDK 45nm technology at different global clock frequencies and temperatures. The performance of proposed integrated technique is compared with power gating technique in terms of performance metrics like average power and leakage power.From simulation results, it is evident that as temperature increases both average and leakage powers is reduced and the sleepy stack technique outstands in its performance as compared with other techniques.

Keywords: Low Power, Flip-Flop, Power Gating, Clock Gating, Latches.

1. INTRODUCTION

With the small geometries in deep sub-micron technology the number of devices has to be integrated on a single chip, so the devices in a chip and the total power consumption had increases rapidly.

With the increasing popularity of battery driven portable electronics there is a growing demand for low-power circuit designs. With the progress of CMOS technology there is steady growth in clock frequency and chip capacity. So the low power techniques are highly appreciated in current VLSI design. In a CMOS circuit power consumption consists of dynamic and leakage power. Leakage power can be sub-divided into standby and active leakage. Dynamic power consumption occurs in a circuit when it's input toggles. Leakage power is dissipated in a circuit when it's input not toggles is known as standby leakage, so it is referred as the circuit is in sleep mode, while the leakage power consumed in operation mode (when the input toggles) is known as active leakage.

Clock gating (CG) [1]-[5] is the most widely used technique for the reduction of dynamic power in CMOS circuits. Power gating (PG) [6]-[9] is the dominant technique to reduce the standby leakage power. The active leakage power becomes more important, so it is differ from normal PG, the PG to minimize active leakage power in operation mode is referred as a run time power gating [10]-[12]. During the clock gated period there are some components that are performing redundant operations and run time power gating will put these components into sleep. Integration of CG and PG is achieved with simultaneous reduction of dynamic and active leakage power [12]-[16].

In this paper, integration of BSCG and PG will leads to the reduction of dynamic and active leakage power simultaneously. After the BGSC is applied to the design the components performing redundant operations during the clock gated period are determined by forward traversing the circuit from the gated flip-flop outputs. These components will be power gated using the clock enable signal generated by BSCG.

The rest of this paper is organized as follows. Section 2 gives an overview of CG and PG. BSCG is presented in Section 3. Integration of BSCG and PG is explained in Section 4. Simulation results are shown in Section 5 and concluded in Section 6.

2. PRELIMINARY CONCEPTS

2.1 Clock Gating (CG) Basics

As the operating speed increases of a chip then the dynamic power consumption increases dramatically.CG is a technique used to gate the unnecessary clock toggles of a registers. Clock gating is a technique that is used to control the power dissipated by a clock network and it reduces the dynamic power dissipation. In a synchronous circuits clock network is responsible for a power dissipation up to 40%..Clock gating reduces the unwanted switching on the parts of a clock network by disabling the clock signal. Clock gating saves the power by adding a more logic to a clock network. When the clock is not switched the switching (dynamic) power consumption goes to zero and there is only a leakage current is occurred. Clock gating shuts off the clock when the system is in current state so that the dynamic power consumption is reduced.

Fig.1 shows a CG architecture it consists of a signal called activation function (F_a), latch, AND gate and registers. Activation function is defined in order to selectively stop the clocking of the circuit then the activation signal is filtered by a latch when the global clock is high. The purpose of latch is to filter glitches of the activation signal that should not propagate when the global clock is low. When both of the

global clock is and the output of latch are high then the gated clock signal is applying as a clock signal for the registers i.e. when there is change in the input data of a register at that time the gated clock is applying. Activation signal is a combinational block that extracts the information from primary and state inputs of a circuit.

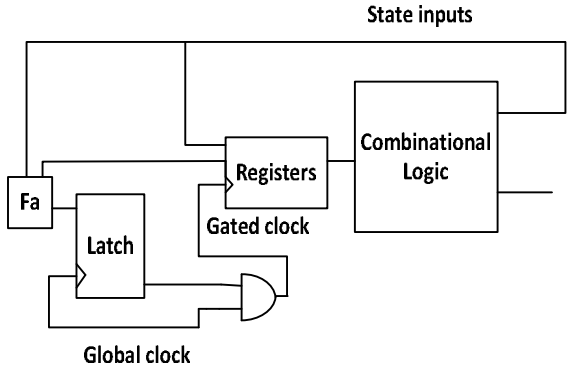

Fig.1. Clock Gating (CG) Architecture

2.2 Power Gating(PG) Basics

As the scaling of MOSFET proceeds leakage power of chip will increases dramatically. Leakage power is the major concern in portable devices because it wastes the energy in standby mode and leads to shortening of battery life. So one of the effective techniques to reduce the standby leakage is power gating in which power switches (sleep transistors) are inserted among logic circuits, power supply and ground. Power switch is turned off when the system is in standby mode so that the power is off for the system so the leakage current is reduced.

PG is also called as MTCMOS technique in which the header (PMOS) and/or footer (NMOS) transistor is inserted on the pull-up and/or pull-down network of a CMOS gate. The transistors are turned off when the circuit is in standby mode thus reducing the leakage current that flows from supply to ground path shown in fig.2. The power switches are normally referred as sleep transistors because they are driven by the same signal. In a power gated design sleep transistors controls the clusters of gates instead of individual gates.

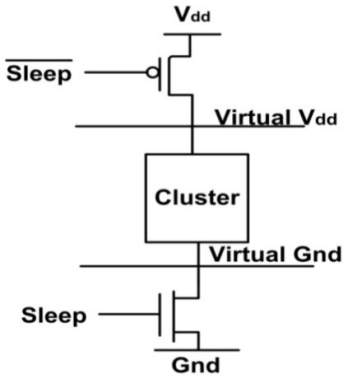

Fig.2. Power Gating (PG) Architecture

3. BUS SPECIFIC CLOCK GATING (BSCG)

It is used to reduce the dynamic power and it can be realized by D-flip-flops, AND, XOR and OR gates. BSCG circuit compares the inputs and outputs and gates the clock when they are equal i.e. when there is change in the input data of gated FFs then only the gated clock is applying for D-FFs otherwise the gated clock signal is not applying. Fig. 3(a) shows a non-clock gating circuit and fig b shows a BSCG circuit.

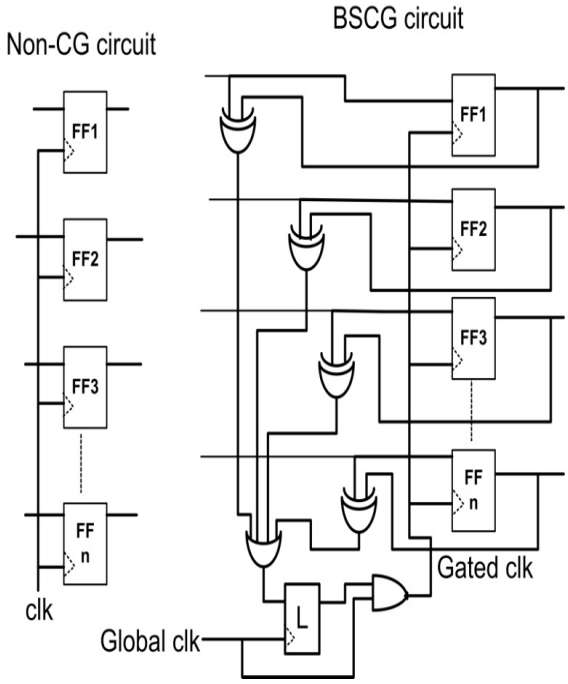

Fig. 3(a) Non-clock gating circuit (b) BSCG circuit

4. INTEGRATION OF BSCG AND PG

A footer power switch is inserted either in between actual ground and virtual ground of the power gated cells or a header switch is inserted in between power supply and the virtual power supply of power gated cells are shown in Fig. 4. The enable signal generated from BSCG is used as sleep signal for PG cells. PG cells are totally dependent on gated FF outputs. Holders are placed in between the power gated cells and the non-power gated cells so that non-power gated cells can function properly.

Integration of BSCG and PG can be explained in detail by considering an example of synchronous circuit as shown in Fig. 5. It consists of four out of five FFs are clock gated. For it first we had applied BSCG technique then four FFs are clock gated. The dashed lines are completely dependent on stable gated FFs outputs, so they are inactive and can be power gated into sleep. However, one input of the xor gate H is the output of un-gated FF1, since it may not be stable (active) during clock gated period. In order to avoid floating signal, holder logic is placed at the output of power gated cell if that output connects to non-power gated cells or primary outputs.

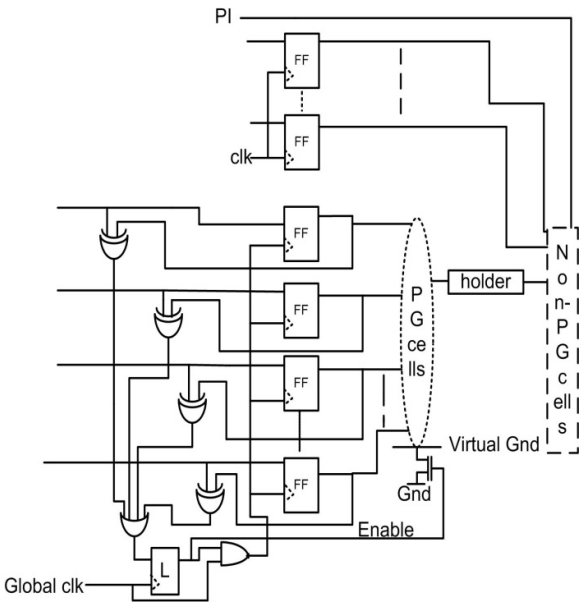

Fig. 4. Integration of BSCG and PG

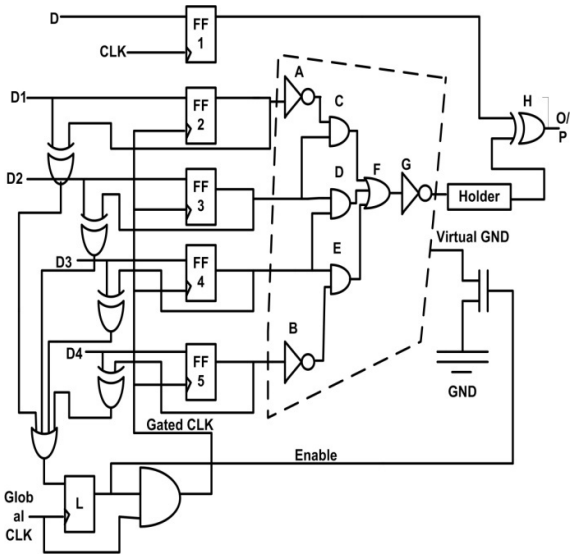

Fig. 5. Synchronous circuit example

5. RESULTS

The synchronous circuit is simulated in CADENCE 45nm technology. Average power and leakage power with different power gate techniques at different global clock frequencies and at different temperatures are shown in Table 1 and there variations with temperature are shown in the figures6 - 9 for average power and in figures 10 - 13 for leakage power.

Table 1: Average power and Leakage Power

Power Gating Schemes	Average and Leakage Powers (nW) at-27^{0}C			Average and Leakage Powers (nW) at 0^{0}C			Average and Leakage Powers (nW) at27^{0}C			Average and Leakage Powers (nW) at50^{0}C		
	Global Clock Frequencies			Global Clock Frequencies			Global Clock Frequencies			Global Clock Frequencies		
	20MHz	25MHz	50MHz	20MHz	25MHz	50M Hz	20MHz	25MHz	50MHz	20MHz	25MHz	50M Hz
Dual Sleep Technique	968.2	1008	990	888.6	927	914.6	823.4	860.3	852.8	778.4	814	810.6
	625.5	684.7	630.9	602.3	631.6	576.8	573.4	599.2	544.3	535.9	559.9	503.1
Sleep Technique	965.2	1005	987.3	883.1	921.4	909.6	821.9	858.9	850.4	776.8	812.7	808.2
	622.3	677.4	624.1	598.9	626.6	574.2	573.9	600	544.6	536.9	560.7	503.4
Stack Technique	960.9	1002	985.9	879.4	919.8	905.8	817.7	856.7	849.3	776.2	812.5	808
	618.5	668.3	622.2	595.2	624.5	570.6	570.5	598.2	543.2	533.7	557.8	501.1
Sleepy Stack Technique	958.7	999	981.5	876.5	914.9	902.2	816	852.3	844.3	771.7	808.4	803.6
	615.8	664.9	618.6	589.3	619.8	565.4	569	594	538.7	532.7	556.2	498.2

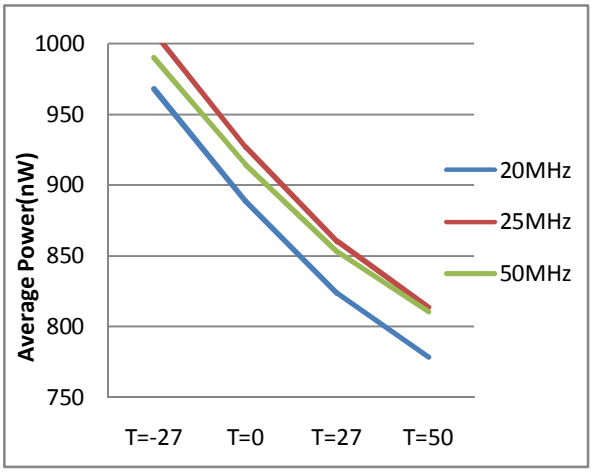

Figure6: Average power versus temperature for Dual Sleep Power Gating Technique

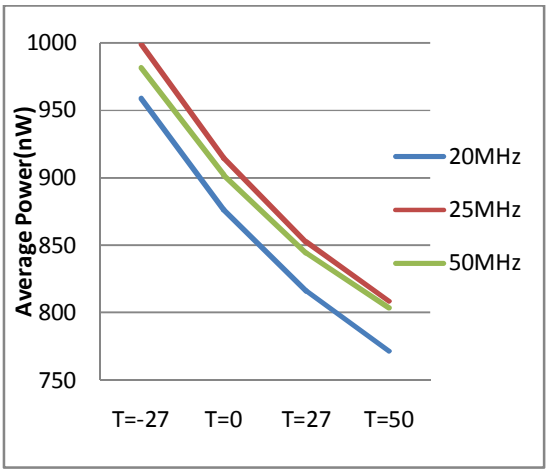

Figure9: Average power versus temperature for Sleepy Stack Power Gating Technique

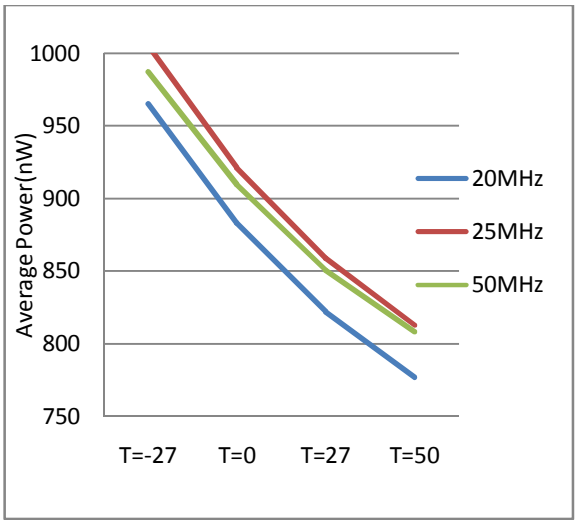

Figure7: Average power versus temperature for Sleep Power Gating Technique

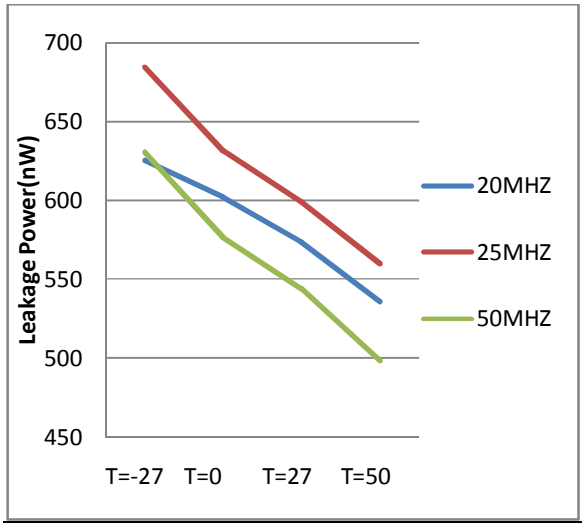

Figure10: Leakage power versus temperature for Dual Sleep Power Gating Technique

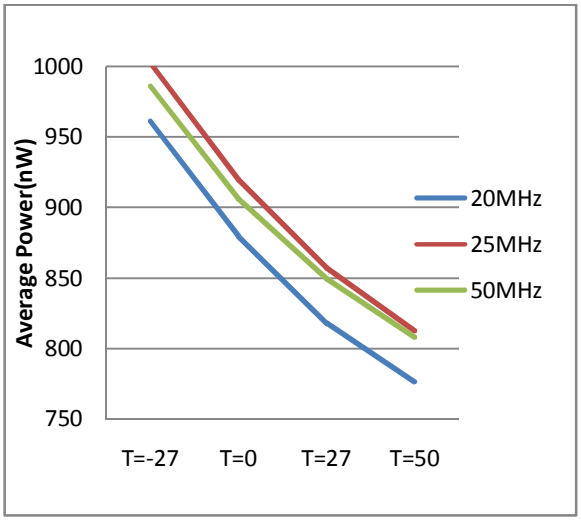

Figure8: Average power versus temperature for Stack Power Gating Technique

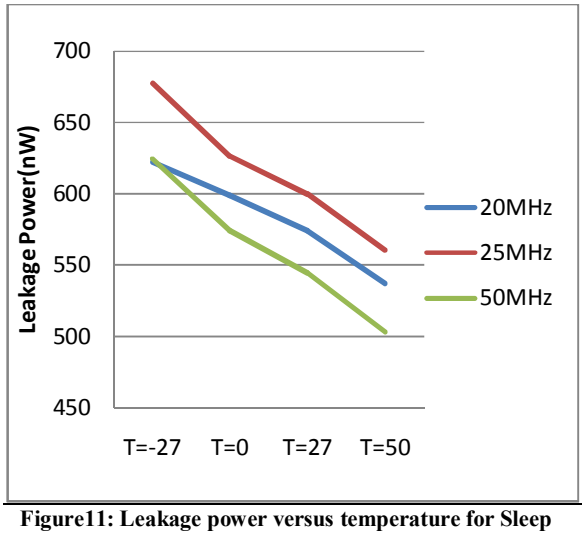

Figure11: Leakage power versus temperature for Sleep Power Gating Technique

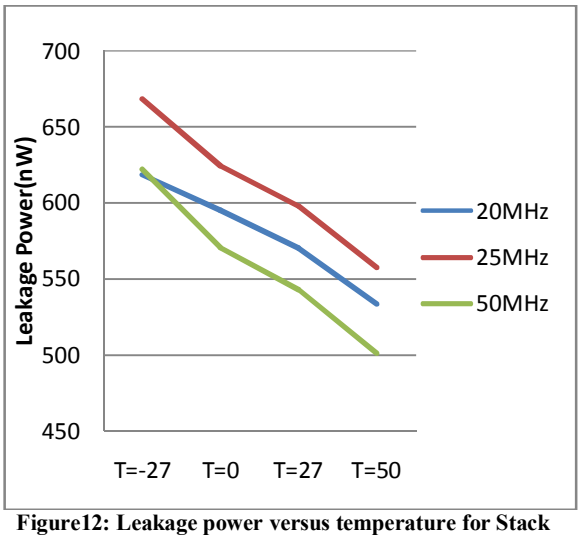

Figure12: Leakage power versus temperature for Stack Power Gating Technique

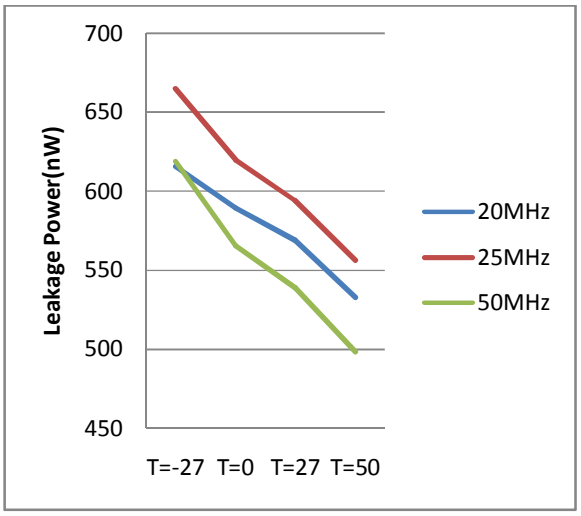

Figure13: Leakage power versus temperature for Sleepy Stack Power Gating Technique

6. RESULTS

In this paper an integration of BSCG and PG is achieved in sequential circuits. First BSCG technique is evaluated it selects the flip-flops for gated and the clock enable signal generated from BSCG used as sleep signal in PG. A synchronous circuit is implemented by using both BSCG and PG and there average power and leakage power are evaluated by power gating techniques at different global clock frequencies and at different temperatures. As Temperature increases both average and leakage powers are reduced and the best method is sleepy stack.

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