Design and Implementing Novel Independent Real-Time Software Programmable DAQ System using Multipurpose MCU and Sigma Delta

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Abstract: The crucial features of many demanding applications like industry and aerospace are data acquisition and telemetry. It is vital to observe and analyse the real time performance, in launch vehicle systems, so that designs can be certified and tuneablefactors could be regulated to intensification the act and competence. At present used DAQ structures are of augmented size, weight and turn out to be exorbitant and power hungry. This article introduce a new mission-independent real time software programmable DAQ system using multipurpose MCU and sigma delta ADCs are planned, taking into account size, weight, costand act without compromiseon precision, firmness and drift act. Additional digital filtering steps are also added to progress the system act. This system isproficientfor directconnectionswithdiverse pressure and temperature sensors which interfaces 32 low frequency channel and two high frequency channels. The system planned operates in two modes; one is data acquisition modules is also affected upon as avenues for future work.

Keywords: Data acquisition system; Digital filter design; Versatile systems; wireless protocol; sigma delta

1. INTRODUCTION

A Data acquisition (DAQ) system in common involves of sensors, DAQ measurement hardware and a computer with programmable software. Compared to customary measurement system, PC based DAQ systems explicit the processing power, productivity display and connectivity abilities of industry standard computers providing a more powerful, flexible and cost effective measurement solutions. The sensors are the transducing elements, may want electrical excitation in the form of voltage or current, and are provided by the DAQ system. The DAQ systems and Telemetry systems have advanced substantially over the years and being used to collect real time data from sources in order to aid observing, analysis, and control facility [1, 2]. For this purpose the flight transmitted telemetry data is received and put in storage in the ground station. The data of the earlier mission forms a vital and important source for the analysis and design in later missions.

Current data achievement system considers only 16 low frequency channels and is controlled by an eight bit microcontroller of PIC18F6xxx family. Our necessity is to produce a well-organized system with reduced size and weight which meet the signal conditioning and data acquisition necessities of launch vehicle telemetry, without compromising on precision and determination. Adjusting the current system with the existing microcontroller will increase the extent and weight of the system and it possess peripheral and I/Oconfines too. This revision describes the design of a data acquisition system based on 16-bit PIC microcontroller

of PIC24EPxxx family and sigma delta Analogue to Digital Converter's (ADCs) of ADS1218 and ADS1255 [3, 4] .The planned system interfaces directly with sensors accepting their low level analogue signal as input in case of ADS1218 and high level analogue signal as input in case of ADS1255.ADCs related with each channel performs the required signal conditioning. The gain and anti-alias filter cut-off frequency are set by the substances of control registers on the chip. The major factors of signal conditioning such as gain ,input signal offset and anti-alias filter cut-off frequency are digitally controlled, thus rendering the system versatile and reconfigurable. There are two modes of performance. One is program mode and another is data acquisition mode. The program mode purposes include writing to ADC's configuration registers and reading from these registers to confirm the integrity of data. Other purposes such as reset, selfcalibration, system gain and system-offset calibration are also applied in this mode. In data acquisition mode, the system obtains the digital data from the ADC and posts the proper data to Data Processing Unit (DPU). Use of one extra RS-485 link in the output for check out purpose, is also reviewed as another major feature of this system. Overview of Digital filtering phases using moving average concepts also improves the efficiency of the system.

The block diagram illustration of complete system with a brief explanation, and timing details are debated in section II. The software association including modes of operations and flow diagram are defined in section III. Performance details and consequences are discussed in section IV. Section V accomplishes the work and brings out an overview for additional enhancements in the system capabilities.

2 .DESIGN DETAILS

2.1 Block Diagram Explanation

The hardware association of the system is shown in the fig.1. The planned system edges 32 –low frequency channels and two high frequency channels. Each channel contains of 24-bit sigma delta ADC of ADS1218 in case of low frequency channels and ADS1255 for high frequency channels [3, 4]. Whole system is controlled by a single 16-bit microcontroller of PIC24EP512GU814 and these microcontrollers feature built-in flash memory for program storage, Random Access Memory (RAM) for data buffering and support of a diversity of standard edges such as Serial Peripheral Interface (SPI) and Universal Asynchronous Receiver Transmitter (UART). The output interface is electrically well-suited to industry standard RS-485 and makes use of three MAX3443 devices for redundant observing. The ADCs are arranged and read by the microcontroller through the SPI port and here the digital output from each channel is read and written on to the Data RAM inside the microcontroller. The data matching to each channel is then communicated to a downstream DPU over RS485. Communication over RS-485 bus is controlled through the UART port. Supporting circuits like Power-On- Reset (POR) and Voltage Reference Generators are also comprised to the hardware, to make it more efficient.

2.2 Timing Information

In usual operational mode the microcontroller polls the channels sequentially for data readiness. The order of polling can be as per a format deposited in memory. The edge between microcontroller and ADC is by means of the standard Serial Peripheral Interface (SPI). The communications over the SPI port are synchronised via a Serial Clock (SCLK) of 1MHz initiate by the microcontroller [5, 6]. The ADS1218 will cater to all low frequency quantities up to 60Hz bandwidth and have a master clock rate of least 1MHz and maximum 5MHz. ADS1255 channels are used for high frequency quantities up to 1.06 KHz bandwidth and have a master clock rate of least 0.1MHz and maximum 8MHz. The communication done by the RS-485 bus foll ows the standard asynchronous communication protocol. When command from DPU arrives, the command is send to the DAQ unit over RS-485 bus, which is arranged in half duplex multi drop bus format. Then each unit decodes the address and the one whose base address equals the command word sends back a reply word to the DPU. The communication over RS485 output edges are based on the precedence, interrupt driven mode controlled by the microcontroller unit (MCU). The MCU is arranged in external crystal oscillator mode with an operating frequency of 16MHz so that equivalent instruction rate of 8MIPS (Million Instructions per Second). The Universal asynchronous Receiver Transmitter (UART) provisions a baud rate of 2MBPS. The UART commands are of 11 bits which needs 0.5 µs for each bit transmission. The signalling rate of 2MBPS supported by the transceiver will ensures that the output port can tolerate a combined throughput of 1 data samples in every 32 microseconds [7, 8].

3. SOFTWARE SPECIFICS

The Integrated Development Environment (IDE) is an atmosphere which integrates dissimilar simulation tools and compilers to provide a single window solution to development and debugging. MPLABV8.92 is an IDE delivered by the microchip,

3.1 Program Mode

Functions such as reset, self-calibration, system- offset and system-gain calibration are applied in this mode based on the

commands FE, F0, F3 and F4 correspondingly. The RS-485 interface itself can be utilized to load the formation data for each channel. The programming of ADC chip is an off-line operation and it is arranged in such a manner as to load this data automatically in power-up onto its arrangement registers. These ADCs have diverse gain values and is based on the internal reference voltage and differential input voltage of the ADC. Diverse gain settings of ADC are revealed in Table 1.

Table 1. Gain sets of ADC

V ref	Differential input Voltage variety	Gain
2.5V	0-2.5V	1
2.5V	0-1.25V	2
2.5V	0-0.625V	4
2.5V	0-312.5mV	8
2.5V	0-156.25mV	16
2.5V	0-78.125mV	32
2.5V	0-39.0625mV	64
2.5V	0-19.53mv	128
1.25V	0-10mV	128

3.2 Data Acquisition Type

In this approach, the ADCs are polled constantly. The 16-bit data is read from ADC and deposited in the data memory of microcontroller. It is conceivable through SPI routine and this process constant until the microcontroller receives a command from DPU. This command demand is controlled using interrupts and the interrupt service routine manages the posting of reply to DPU. It is conceivable through UART routine. After sending the reply, the microcontroller proceeds to ADC polling.

3.3 SPI routine

The communication between MCU and ADC is conceivable through SPI through five hand shaking signals, the Chip Select (CS), Data Ready (DRDY), SCLK (Serial Clock), Data Input (DI) and Data Output (DO) lines. The separate ReaDY (DRDY) signal corresponding to each chip is used to check the data legitimacy before reading the corresponding channel. The CS lines are separately supplied to each chip when equivalent channel is to be accessed. The data handover is synchronised with a SCLK of 1MHz. The microcontroller polls channel serially, selects the ADC if data is ready, issues a Read Data (RDATA) command and reads the data over the SPI port.



Figure.1 Block diagram of a 34-channel data acquirement scheme

3.4 Title UART routine

In the output, the microcontroller is interfaced to the DPU over UART. The UART uses the standard Non-Return –to-Zero (NRZ) format with one start bit, 8 data bits, 1 mode bit and one stop bit. The flowchart for UART routine is revealed in fig.2. The mode bit is used to distinguish between command and reply. The command order from DPU and the reply sequence from DAU (Data Acquisition Unit) in the RS-485 protocol are revealed in fig.3 and fig.4 correspondingly.



Figure.3 command order from DPU



Figure.4 Reply order from DAU



Figure .2 UART routine.

3.5 Filtering phase

A digital filter at the input of ADC using moving average notions increases the competence of the system. This simple low-pass filter creates an ADC with enhanced resolution and thus the system become more efficient. The Effective number of bits (ENOB) in an ADC can be considered using the equation 1.

$$ENOB = Log 2 \left(\frac{Vref}{3 * S \tan dardDeviation} \right)$$
(1)

• ENOB=Effective Number of Bits

4. CONCLUSION

In Data Acquisition method, the ADCs channels are polled constantly and the available data is read and stored in the memory of microcontroller. This system continuous until it receives a command from DPU. The command demand is managed using interrupts and interrupt service routine handles the posting of reply to DPU. The simulation consequences for SPI and UART routine in data acquisition method are shown in fig.5 and fig.6 correspondingly.

The program is verified in the demo board of PIC24E series. The board delivers a low-cost, modular expansion system for Microchip's enhanced 16-bit Digital Signal Controllers (DSCs) or High-Performance Microcontrollers (MCUs). It also comprises of crystal oscillators, Green power indicator LED, USB connectivity for on-board debugger communications, three push button switches (SW1, SW3) for user-defined inputs, Three user-defined indicator LEDs (LED1, LED2, LED3), USB Type A connectivity for dsPIC33E/PIC24E USB host-based applications, Host mode power jumper and a Regulated +3.3V power supply for cause to move the starter kit via USB or an development board.

5. CONCLUSION AND UPCOMING WORKS

Data acquisition and telemetry is fragment of winning formula of many arenas comprising industry and aerospace. The carrying out of competent software programmable real time data acquisition system with limited size and weight is debated in this work. It outcomes in an efficient system in terms of sigma-delta ADCs, that can deliver higher input signal bandwidth and the

digital filter placed at the input of ADCs, which yields betterquality resolution. The adaptability of the system in terms of software reconfiguration, calibration and sensor interface extends its application.

Effort is on track of refining the system performance by considering power reduction concepts. Overview of a wireless protocol between diverse data acquisition module will also advance the performance [9].

E File Registers						File Registers			1 Watch						
Address	00	02	04	06	08	0A	0C	0E	Address	00	02	AddSFR	ACLKCON: •	Add Symbol _SP	
10F0	0000	0000	0000	0000	0000	0000	0000	0000	20E0	0000	0000	Update	Address	Symbol Name	Value
1100 1110	FEEA	FFE I FEAB	F3F2 FEAC	FFFE	FYEB FEA7	FREC	FFED FEA9	FFLA FE14	2020	0000	0000		0224	U1TXREG	, 0x0000
1120	FE12	FEIA	FE2B	FF3B	FF4C	FF5D	FF6A	FE7A	2110	0000	0000		1002	j TMR1	0x000B
1130 1140	FE8B	FE9C	FA53	FA5B	FE17	EE27	FE47	FE57	2120	0000	0000		0248	SPI1BUF	0x0001
1150	ETE3	0000	0000	0000	0000	0000	0000	0000	2130	0000	0000		0268	SPI2BUF	0x0001
Hex Symb	Hex. Symbolic Dual Port					Hex Symbolic Dual Port				02AB 02CB	SPI4BUF	0x0001 0x0001			

Fig.5 Polling procedure and reception of command by the microcontroller

💷 Watch				II Watch						
Add SFR SPI2BUF Add Symbol _SP Add SFR SPI2BUF Add Symbol _SP										
Update	Address	Symbol Name	Value	Update	Address	Symbol Name	Value			
	0224	U1TXREG	0x00AD		0224	U1TXREG	0x00FE			
	1002	j	0x0016		1002	j	0x0016			
	0100	TMR1	0x0000		0100	TMR1	0xFFA7			
	0800	IFSO	0x0800		0800	IFSO	0x0800			
	0248	SPI1BUF	0x0001		0248	SPI1BUF	0x0001			
	0268	SPI2BUF	0x0001		0268	SPI2BUF	0x0001			
Watch 1	Watch 2 Watch 3	Watch 4		Watch 1 Watch 2 Watch 3 Watch 4						

Fig.6 Transmission of vital data requested by the DPU

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