

# ASIC Design of Reversible Multiplier Using Adiabatic Technique

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**Abstract**—From past few decades, VLSI technology has been growing to the large extent. All credit for this goes to the increasing usage of integrated circuits for every embedded system, mobile technologies, computing systems, etc. Growth and use of technology has increased the thirst for low energy or power consumption. An Adiabatic approach is perfect solution for the designing of power and energy efficient designs. The word ‘Adiabatic’ is the change of state that occurs without the loss or gain of heat. Reversible computing performed on Toffoli gate having adiabatic design techniques promises more reduced in power consumption as compared to traditional adiabatic CMOS circuits. Tanner EDA tool is used for designing the schematic and analysis. S-EDIT is used to design the schematic and T-SPICE is used to Simulate and check the results of Power Dissipation. W-EDIT is used to display the simulation results in the form of waveform.

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## 1. INTRODUCTION

The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integration technologies and large systems design. Use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. Advances in device manufacturing technology allow steady reduction of minimum feature size (such as minimum channel length of a transistor or an interconnect width realizable on chip). In 1980, at the beginning of the VLSI era, the typical minimum feature size was 2  $\mu\text{m}$ , and a feature size of 0.3  $\mu\text{m}$  was expected around the year 2000. A minimum feature size of 0.25  $\mu\text{m}$  was achieved by 1995. When we compare integration density of integrated circuits, a clear distinction which is made between the memory chips and logic chips. The number of transistors per chip has continued to increase at an exponential rate over last three decades, effectively confirming “Gordon Moore’s” prediction on the growth rate of chip complexity, which was made in the early 1960s (Moore’s Law). It has been observed that in terms of transistor count, logic chips which contain significantly fewer transistors in any given year mainly due to large consumption of chip area for complex interconnects. Today we are going through an advanced IC technology. In this we have VLSI technology.

CMOS is referred to as Complementary Metal Oxide Semiconductor, CMOS technology is becoming the mainstream fabrication technology for memories and microcomputers is only because of its high density and low power features. CMOS is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and various digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transreceivers for many types of communication. But some applications such as computer and communication systems require better speed performance than that

obtained by CMOS technology so bipolar LSI’s have been used in such fields.

## 2. LITERATURE REVIEW

Since last few decades the main challenges were Area, cost, and performance. But these days power is an important factor instead of cost, performance and area. The device which consumes very less power irrespective of speed such as heart pacemaker, RFID etc. works on the principle of adiabatic logic. The aim of reduction in power consumption is application specific. The authors have tried to decrease the power by combining the adiabatic and reversible technique[1]. The power consumed in traditional CMOS design can be given as,

$$P = CL \cdot VDD^2 \cdot f \quad [6]$$

Here the power (P) is proportional to switching frequency (f), capacitance (CL), and square of supply voltage (VDD). Power consumption can be reduced by minimizing power supply, capacitance and switching frequency of operation. But as soon as these parameters reduces, it may deteriorate the performance of the circuit.

Design using adiabatic principle helps in reducing power consumption at the cost of reduced performance. A method based on adiabatic technique uses an ac power supply rather than dc for energy recovery. Theoretically adiabatic circuits

consume zero power, it shows energy loss due to nonzero resistance in the switches. There are so many papers which describe different types of adiabatic technique such as ECRL, 2PASCL, PFAL etc. by which we can reduce power consumption of the circuit [2]. These technique consume less power as compare to other CMOS circuits

### 3.CONCEPTS

#### I.Adiabatic Circuits

The term “adiabatic” refers to the thermodynamic process that exchanges no energy with environment, and therefore there is no occurrence of power or energy dissipation . During the switching process, adiabatic technology reduces the power or energy dissipation and reuses some part of the energy by recycling it from the load capacitance.

Adiabatic circuits are basically low power circuits which use to conserve the energy by returning back its output energy to input, so that the same energy can be used for next operation.

Fig. 1 and Fig. 2 shows the Charging and Discharging in conventional CMOS circuit and Adiabatic System.

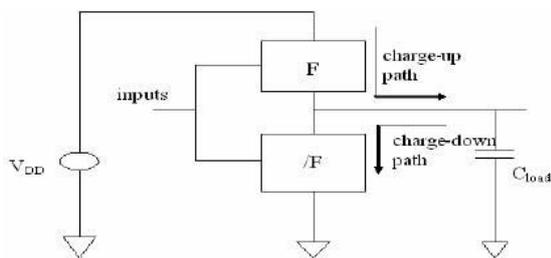


Figure 1. Charging and Discharging in Conventional System

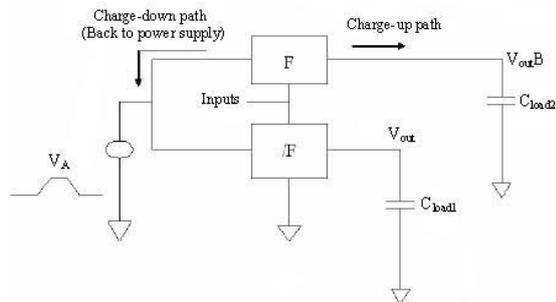


Figure 2. Charging and Discharging in Adiabatic system

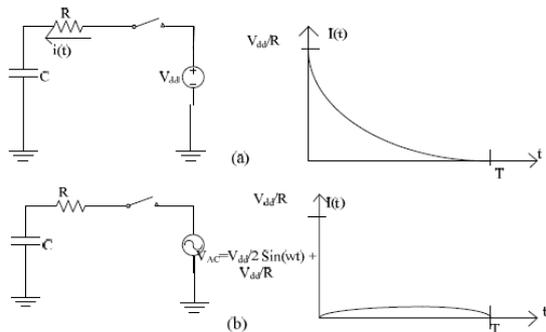


Fig. 3. (a) Switching of CMOS (b) Switching of Adiabatic Logic.

Adiabatic circuits aims to conserve the charges by following essential rules,

- 1) Avoiding turning on of transistor whenever there is a potential difference across the drain and source ( $V_{DS} > 0$ ).
- 2) Avoiding turning off of Transistor whenever there is a flow of current through drain and source. ( $I_{DS} \sim 0$ ).
- 3) The current should not pass through diode.

#### Adiabatic Logic Types

During literature survey, we found different types of adiabatic circuits . They can be grouped into two fundamental kinds:

- Fully Adiabatic Circuit
- Partially energy recovery Adiabatic Circuit (Quasi)

Partially Adiabatic families include the following

- Efficient Charge Recovery Logic
- 2N-2N2P Adiabatic Logic
- Positive Feedback Adiabatic Logic
- NMOS Energy Recovery Logic
- Clocked Adiabatic Logic
- True Single-Phase Adiabatic Logic

### II.Reversible Gates

#### Goals of Reversible Logic:

**A. Quantum Cost:** Quantum cost of a circuit is measure of implementation cost of quantum circuits. More precisely, quantum cost is defined as number of elementary quantum operations needed to realize a gate.

**B. Speed of Computation:** The time delay of circuits should be as low as possible as there are numerous computations which have to be done in a system involving a quantum processor; hence speed of computation is very important parameter while examining such systems.

**C. Garbage Outputs:** Garbage output are those output signals which do not take contribution in driving further blocks in that design. These outputs become redundant as they are not required for computation at later stage. The garbage outputs make the system slower; hence for better efficiency it is very necessary to minimize number of garbage outputs.

**D. Feedback:** Looping is strictly prohibited when we are designing reversible circuits.

**E. Fan-out:** The output of a certain block in the design can only drive at most one block in design. Hence it can be said that the Fan-out is restricted to 1.

Feynman gate (FG) and Toffoli gate (TG), are universal reversible gate. FG shown in Fig.2.1 has QC equals 1 and hardware complexity is  $1\alpha$ . TG shown in Fig. 2.2 has QC equals 5 and hardware complexity is  $1\alpha + 1\beta$ .

#### 2.1 Feynman Gate

It is a  $2 \times 2$  Feynman gate . The input vector is  $I(A, B)$  and output vector  $O(P, Q)$ . The outputs are defined by  $P=A,$

$Q=A\oplus B$ . Quantum cost of a Feynman gate is 1. Figure 2.1 shows a 2\*2 Feynman gate..

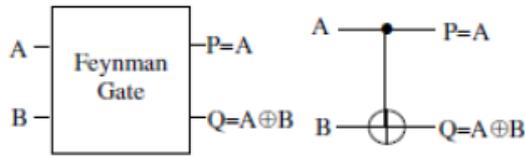


Figure 2.1: Feynman Gate

### 2.2 Toffoli Gate

It is a 3\*3 Toffoli gate . The input vector I(A, B, C) and the output vector O(P,Q,R). The outputs are defined by  $P=A$ ,  $Q=B$ ,  $R=AB\bar{C}$ . Quantum cost of a Toffoli gate is 5. Figure 2.2 shows a 3\*3 Toffoli gate.

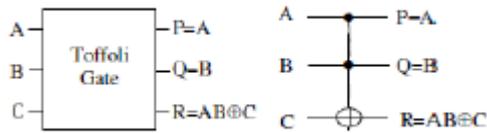


Figure 2.2: Toffoli gate

### Reversible Multiplier

Multiplier circuits are divided into two types : unsigned and signed. Several approaches have been presented to multiply signed numbers, such as 2's complement, Baugh-Wooley, and modified Baugh-Wooley methods . In modified Baugh-Wooley method, number quantity is considered as 2's complement and shows how the multiplication operation takes place, which need AND gates and NAND gates to produce a signed multiplier.

### III.Wallance Tree Multiplication Algorithm

The well-known Wallace high-speed multiplier use carry save adders to reduce an N-row bit product matrix to an equivalent two row matrix that is then summed with carry propagating adder to give product .

The common multiplication method is “add and shift” algorithm. Multiplication algorithm for an N bit multiplicand by N bit multiplier is shown below:

$$\begin{array}{r}
 A = A_3 A_2 A_1 A_0 \text{ Multiplicand} \\
 B = B_3 B_2 B_1 B_0 \\
 \text{Multiplier} \\
 \hline
 Y = Y_7 Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 Y_0 \\
 \text{Multiplication of A and B}
 \end{array}$$

	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Inputs
x	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	
	C	B <sub>0</sub> x A <sub>3</sub>	B <sub>0</sub> x A <sub>2</sub>	B <sub>0</sub> x A <sub>1</sub>	B <sub>0</sub> x A <sub>0</sub>
+	B <sub>1</sub> x A <sub>3</sub>	B <sub>1</sub> x A <sub>2</sub>	B <sub>1</sub> x A <sub>1</sub>	B <sub>1</sub> x A <sub>0</sub>	
	C	sum	sum	sum	sum
+	B <sub>2</sub> x A <sub>3</sub>	B <sub>2</sub> x A <sub>2</sub>	B <sub>2</sub> x A <sub>1</sub>	B <sub>2</sub> x A <sub>0</sub>	
	C	sum	sum	sum	sum
+	B <sub>3</sub> x A <sub>3</sub>	B <sub>3</sub> x A <sub>2</sub>	B <sub>3</sub> x A <sub>1</sub>	B <sub>3</sub> x A <sub>0</sub>	
	C	sum	sum	sum	sum
	Y <sub>7</sub>	Y <sub>6</sub>	Y <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>
	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>		Outputs

For the Wallace reduction method, once partial product array is formed, adjacent rows are collected into nonoverlapping groups of three. Each group of three rows can be reduced by 1) applying a full adder to each column that contains three bits, 2) applying half adder to each column that contains two bits, and (3) passing any single bit columns to next stage without processing.

This reduction method is applied to each successive stage until two rows remain. The final two rows are summed with a carry propagating adder.

### 4.CONCLUSION

It can be seen that the performance of digital circuits can be enhanced using reversible gates. Adiabatic circuits are low power circuits which use to conserve the energy . Reversible multiplier designed using reversible gates and adiabatic logic families reduces power dissipation and leakage current. Wallace approach will minimize the number of required half adder and full adder which will reduce area of circuit.

### REFERENCES

- [1] Gaurav Kumar , Trailokya Nath Sasamal “Design and Analysis of Toffoli gate using Adiabatic Technique” International Conference on Computing, Communication and Automation (ICCCA2015) ISBN:978-1-4799-8890-7/15/\$31.00 ©2015 IEEE.
- [2] Sakshi Goyal , Gurvinder Singh, Pushpinder Sharma “Variation of Power Dissipation for Adiabatic CMOS and Conventional CMOS Digital Circuits” 2ND INTERNATIONAL CONFERENCE ON ELECTRONICS AND COMMUNICATION SYSTEM (ICECS 2015) 978-1- 4788-7225-8/15/\$31.00 ©2015 IEEE.

- [3] Arpan Chaudhuri, Mamia Saha, Moumita Bhowmik “Implementation of circuit in Different Adiabatic Logic” 2ND INTERNATIONAL CONFERENCE ON ELECTRONIC AND COMMUNICATION SYSTEM(ICECS 2015) 978-1-4788-7225-8/15/\$31.00 ©2015.
- [4] P. Rajashekhar Reddy, S. Raghavendra Swami, S. Ravi Kumar “Implementation of High Speed Low Power Combinational and Sequential Circuits using Reversible logic” International Journal of Electrical, Electronics and Computer Systems (IJEECS) ISSN (Online): 2347- 2820, Volume -3, Issue-12 2015.
- [5] A.A. Hatkar, A.P.Hatkar, N.P. Narkhede “ASIC Design of Reversible Multiplier Circuit International Conference on Electronic Systems, Signal Processing and Computing Technologies 978-1- 4799-2102-7/14 \$31.00 © 2014 IEEE.
- [6] B.Dilli Kumar and M. Bharati “Design of energy efficient Arithmetic circuits using charge recovery Adiabatic logic” International journal of engineering Trends and Technology, Volume 4, Issue 1, pp.31-40, April 2013.
- [7] Kartikeya Bhardwaj, Pravin S. Mane, Jorg Henke “Power- and Area-Efficient Approximate Wallace Tree Multiplier for Error-Resilient Systems” 15th International Symposium on Quality Electronic Design 978-1-4799-3946-6/14/\$31.00 ©2014 IEEE.
- [8] Yogesh M. Motey, Tejaswini G. Panse “Hardware Implementation of Truncate Multiplier Based on Multiplexer Using FPGA” International Conference on communication and Signal processing (ICCSP) ISBN 978-1-4673-4866-9 © 2013.
- [9] Ron S. Waters, Earl E. Swartzlander “A Reduced Complexity Wallace Multiplier Reduction” IEEE TRANSACTIONS ON COMPUTERS, VOL. 59, NO. 8, AUGUST 2010.
- [10] Sung-mo Kang, Yusuf Leblebici “Cmos Digital Integrated Circuit’s Analysis And Design” Tata McGraw-hill Third Edition- 2008.
- [11] Douglas A. Pucknell “Basic Of VLSI Design” Prentice-hall, Inc., 2007.
- [12] Neil H.E. Waste, David Harris., Ayan Banerjee, “Principles Of CMOS VLSI Design- A Circuit And Systems Perspective”, Third Edition, Addison-Wesley, MA, May 2004.