International Journal of Computer Applications Technology and Research
Volume 12–Issue 03, 22-25, 2023, ISSN:-2319–8656
DOI:10.7753/IJCATR1203.1006

Design of a Wide Input Voltage Low Quiescent Current LDO

Tianfu Li
School of Communication Engineering
Chengdu University of Information Technology
Chengdu, China

Fengbo Wang
School of Communication Engineering
Chengdu University of Information Technology
Chengdu, China

Bo Gou
School of Communication Engineering
Chengdu University of Information Technology
Chengdu, China

Abstract: A low-dropout linear regulator (LDO) with wide input voltage range, wide output voltage range and low quiescent current power consumption is proposed, which is applied to the switching power supply chip to power the internal module of the switching power supply chip. The low-dropout linear regulator is based on a P-type PowerFET design consisting of an error amplifier, a Bandgap reference. The circuit was designed and implemented by SMIC 0.18um BCD process, simulated and verified using Spectre software. The simulation results show that the linear regulation is 0.04mV/V in the input voltage range of 3.5-30V, and the load regulation is 1mV/mA in the output load current range of 10uA to 10mA, and the quiescent current is only 10uA.

Keywords: LDO; wide input voltage range; low quiescent current; low-dropout linear regulator; BCD process; wide output voltage range

1. INTRODUCTION

Low-dropout linear regulator (LDO) is a voltage converter with simple structure, low cost and small output voltage ripple, which is widely used in portable wearable devices, high-end medical testing instruments, industrial robot arms and low-power LED lighting fixtures[1]-[3]. The traditional pure CMOS process LDO can support the input voltage range is generally below 5V, which cannot meet the complex input voltage scenarios of modern electronic devices, and mobile electronic devices put forward more stringent requirements for battery life, and the smaller the LDO quiescent current index, the better. For wide input voltage LDO, the design challenge lies in the isolation of high and low voltages to prevent damage to the LDO internal MOSFET during operation. When the LDO supplies power to the internal module of the DC-DC switching power supply in the chip, the power consumption of the oscillator circuit fluctuates by the order of MHz, resulting in a large overshoot of the output voltage. At low quiescent current, there is more reliance on the transient response enhancement structure to reduce overshoot to stabilize the output voltage. Therefore, ensuring a wide input range and low quiescent current, proper function and stable output of the LDO are the keys to designing high-performance wide input and output LDO.

At present, the main research hotpots of LDO focus on low quiescent current, fast transient response, and high power supply rejection ratio for different application scenarios. Literature[4] proposes an error amplifier with dynamic adaptive bias function and a new FVF (flipped voltage follower) structure LDO, designed for 0.8V low voltage application scenarios, the normal operation quiescent current is only 16nA. Literature[5] proposes a multi-loop compensated high-performance LDO, in which the bias current of the difference amplifier and output buffer changes with the load current, and the dynamic current generated by monitoring the output voltage and the voltage of the EA output node is generated to charge and discharge each node of the loop to improve the output transient response of the LDO. Literature[6] proposes a high-efficiency LDO with multiple small gain stages that provide loop gain without introducing low-frequency poles within the closed-loop bandwidth. Therefore, the response speed of the LDO is improved while maintaining the accuracy of the output voltage. Literature [13] proposes a feed-forward ripple cancellation technique to achieve high power supply rejection ratio of wide-range LDO. It achieves a power supply rejection ratio of less than -56dB at 10MHz at 25mA load current.

In this paper, an LDO circuit supporting a wide input and output voltage range is proposed to achieve high and low voltage isolation using the BCD process with very low quiescent current power consumption, this LDO is suitable for powering internal modules of DC-DC switching power supplies. At the same time, it has good power supply rejection ratio performance under the input range voltage, which is enough to effectively reduce the interference of the power supply voltage.

2. THE STRUCTURE AND PRINCIPLE OF LDO

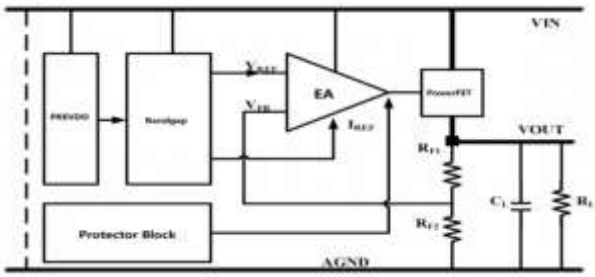

Figure 1. block of LDO

As DC voltage source, the basic principle of a low-dropout linear regulator is to sample the output voltage through an error amplifier and adjust the PowerFET gate control voltage in real time to keep the output voltage stable[7]. The block diagram is shown in Figure 1 and consists of an error amplifier, a PowerFET, a feedback resistor string, a Pre-Buck circuit, a Bandgap reference, and protection module. The Pre-Buck circuit provides a start-up signal and bias current to limit the speed at which voltage and current settle during power-up and avoid circuit instability[8]. A reference reference superimposes

currents or voltages with positive and negative temperature coefficients to produce a zero temperature coefficient current or voltage. The abnormal protection module can effectively avoid the damage of the chip due to over voltage, over temperature and other conditions. Power tubes are used to supply current to the load and are available in N-type and P-type PowerFET, both of which have advantages and disadvantages.

3. CIRCUIT STRUCTURE DESIGN

3.1 LDO Core Circuit

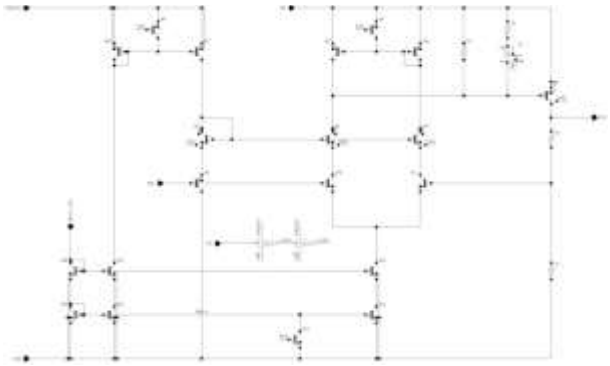

Figure 2. LDO Core Circuit

The core circuit structure of the LDO module proposed in this paper is shown in Figure 2. The circuit includes a bias current mirror composed of M29, M30, M33, M34, M35 MOSFET, error amplifiers composed of M10, M11, M3, M3a MOSFET, and power pass transistors M0. The bias circuit provides the error amplifier with a bias current that guarantees proper operation of the LDO, and the bias current of the error amplifier is set to 6uA for low quiescent current. M2, M77 MOSFET is N-type drain extend MOSFET, source leakage energy high voltage resistance, their role is to isolate high voltage and low voltage, avoid 5V low voltage pipe damage, M6 pipe function is to raise M2, M77 tube bias voltage. The LDO internal error amplifier is a single-stage structure with a high impedance point that introduces a lower frequency pole with a frequency of:

$$P_s = \frac{1}{R_4 \cdot C_{GD,MO}} \quad (1)$$

As can be seen from the above equation, the pole frequency can be set by resistor R4, and C_{GD} and M0 are the power tube gate leakage parasitic capacitance. The pole P_s is the secondary point, the main pole of the LDO is set by an external capacitor, and the main pole frequency is:

$$P_n = \frac{1}{R_{OUT} \cdot C_L} \quad (2)$$

When the load current is larger, the smaller the R_{OUT} resistance, the higher the frequency of the main pole, at which time the frequency of the main pole and the secondary point is closer, which will affect the frequency stability. The stability of the LDO at the output of the main pole decreases as the load current increases.

3.2 Pre-Buck Circuit

Pre-Buck circuit powers the bias circuit and Bandgap references. Since a reference voltage and bias current are required for proper operation of the LDO, a simple power supply circuit is also required before the LDO starts. The Pre-Buck circuit proposed in this article is shown in Figure 3.

Figure 3. Pre-Buck Circuit

The circuit consists of a Zener diode and an N-type drain extend MOSFET, which is a source follower structure, and capacitors C1 and C2 are filter capacitors to reduce output capacitance disturbance. The breakdown voltage of the Zener diode serves as the gate reference voltage of the source follower, and the output voltage of the PREVDD port can be expressed as:

$$V_{PREVDD} = V_{BV,ZDIO} - V_{TH,NDE} \quad (3)$$

Among them, $V_{BV,ZDIO}$ are the Zener diode breakdown voltage, and $V_{TH,NDE}$ are the threshold voltages of N-type drain extend MOSFET. Since the current flowing through the N-type drain extend MOSFET is small, the threshold voltage of the N-type drain extend MOSFET is used to approximate the PREVDD port output voltage.

3.3 Bandgap Reference Circuit

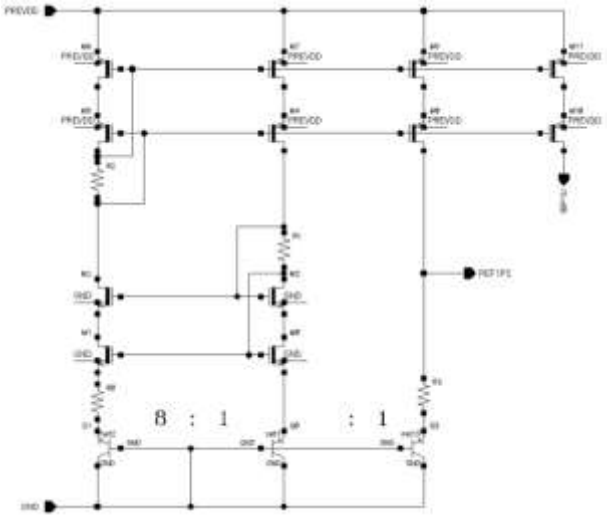

Figure 4. Bandgap Reference Circuit

The Bandgap reference circuit proposed in this paper is shown in Figure 4, Q0-Q1 and M0-M7 form a positive feedback loop with a gain of less than 1, so that the source voltage of M0 and M1 is equal and the emitter currents at both ends of PNP type transistors Q0 and Q1 are also equal, and the emitter currents at both ends are:

International Journal of Computer Applications Technology and Research
Volume 12–Issue 03, 22-25, 2023, ISSN:-2319–8656
DOI:10.7753/IJCATR1203.1006

$$\Delta V_{BE} = V_{BE,Q0} - V_{BE,Q1} \quad (4)$$

$$I_E = \frac{\Delta V_{BE}}{R_0} \quad (5)$$

where $V_{BE,Q0}$, $V_{BE,Q1}$ is the base-emitter voltage of Q0 and Q1, the current is copied from the 1:1 current mirror to the Q2 branch, then the reference voltage is:

$$V_{REF} = R_3 \cdot \frac{\Delta V_{BE}}{R_0} + V_{BE,Q2} \quad (6)$$

The base-emitter voltage of triode is negative temperature coefficient and the voltage is positive temperature coefficient, so zero temperature coefficient reference voltage can be obtained by setting the appropriate proportional relationship between resistors R0 and R3.

4. Simulation results and analysis

The LDO in this paper is designed using the device library of SMIC 0.18um BCD process, which supports 3.5-30V input voltage range, output voltage range 3V-5V, and max load current range 0~10mA.

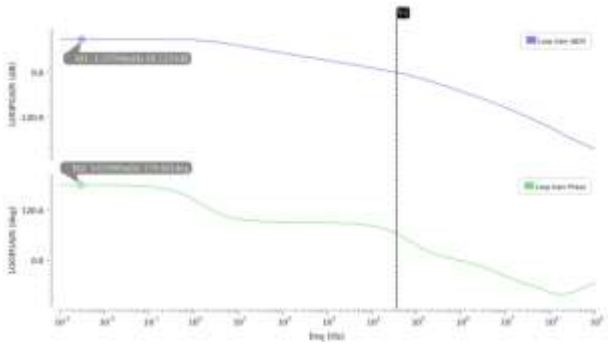

Figure 5. LDO AC Analysis

At the maximum load current, the main pole frequency is highest. At this point, the frequency of the main pole is closest to the secondary pole, and the overall loop stability of the LDO under this condition is the worst case. At 10mA load, the amplitude-frequency characteristic curve is shown in Figure 5. It can be seen that the low-frequency loop has a gain of 88dB and a phase margin of 64°, and the loop remains stable in the worst-case scenario.

Figure 6 and Figure 7 are the simulation results of linear regulation and load regulation, respectively. It can be seen that the input voltage rises from 5V to 30V, the output voltage hardly changes, and the linear regulation rate is excellent. The output load current rises from 10uA to 10mA, the output voltage changes at 1mV/mA, and load regulation is also excellent.

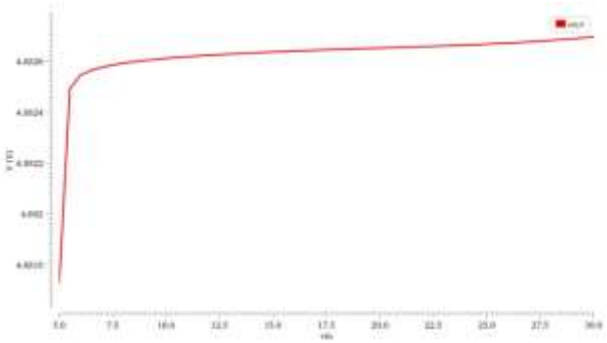

Figure 6. Line Regulation Analysis

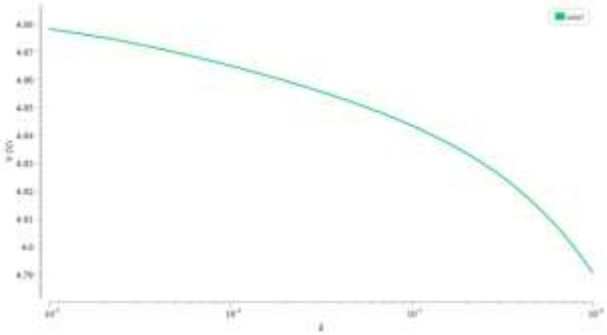

Figure 7. Load Regulation Analysis

A comparison of LDO parameters in this paper with other literature is shown in Table 1. It can be seen that this article has certain advantages in terms of input voltage range, output voltage range, and quiescent power consumption.

Table 1. Comparison of LDO parameters

parameters	[9]	[10]	[11]	This work
Process/nm	250	350	65	180
Input voltage Range/V	3.9-20	1.4-3.3	1.3	3.5-30
Output voltage Range/V	2.5	1.2	1.1	2-5
Max load current/mA	800	50	50	10
quiescent current/uA	800	200	50~190	10

5. CONCLUSIONS

In this paper, a wide input and output voltage range, low quiescent current LDO applied to switching power supply chips, input voltage range of 3.5-30V. linear regulation performance and load regulation performance are good. In the full load current range of 10uA-10mA, LDO can keep the loop stable. Quiescent current consumption is only 10uA.

6. REFERENCES

[1] Akhamal H, Chakir M, Qjidaa H. A 90nm CMOS LDO regulator with high load regulation using a gain boost-up technique[C]// 2016 5th International Conference on Multimedia Computing and Systems (ICMCS). IEEE, 2016.

[2] Yang X, Lu T, Zhang J, et al. A Low-Quiescent Current Low-Dropout Regulator with Wide Input Range. 2014.

[3] Li Z, He L, Chen C. A novel low-dropout regulator with large load current and high stability[C]// 2014 IEEE Workshop on Advanced Research and Technology in Industry Applications (WARTIA). IEEE, 2014.

[4] Adorni N, Stanzione S, Boni A. A 10-mA LDO With 16-nA IQ and Operating From 800-mV Supply[J]. IEEE Journal of Solid-State Circuits, 2020, 55(2):404-413.

[5] Duong Q H, Nguyen H H, Kong J W, et al. Multiple-Loop Design Technique for High-Performance Low-Dropout Regulator[J]. IEEE Journal of Solid-State Circuits, 2017, 52(10):2533-2549

[6] HO M. A Low-Power Fast-Transient 90-nm Low-Dropout Regulator With Multiple Small-Gain Stages[J]. IEEE Journal of Solid-State Circuits,2010,45(11).

[7] Al-Shyoukh M, Lee H, Perez R. A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation[J]. IEEE Journal of Solid-State Circuits, 2007, 42(8):1732-1742.

[8] Hazucha P, Karnik T, Bloechel B, et al. An area-efficient, integrated, linear regulator with ultra-fast load regulation[C]// 2004 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No.04CH37525). IEEE, 2004.

[9] Yin J, Huang S, Duan Q, et al. An 800 mA load current LDO with wide input voltage range[C]// 2017 International Conference on Circuits, Devices and Systems (ICCDS). IEEE, 2017.

[10] Blakiewicz G. Output-capacitorless low-dropout regulator using a cascoded flipped voltage follower[J]. IET Circuits, Devices & Systems, 2011, 5(5):418-423.

[11] Huang M, Feng H, Lu Y. A Fully Integrated FVF-Based Low-Dropout Regulator With Wide Load Capacitance and Current Ranges[J]. IEEE Transactions on Power Electronics, 2019, 34(12):11880-11888.