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Design of a 12 bit SAR ADC with Self-Calibration

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Abstract: Successive approximation analog-to-digital converter (SAR-ADC) are widely used in intelligent sensing fields due to it's low power consumption, medium and high precision and such characteristics. Traditional binary SAR ADC have non-ideal factors such as DAC capacitor array mismatch and comparator offset, which severely limit it's performance. Therefore, a self-calibration method for non-ideal factors is proposed in this work, and theoretical derivation and simulation analysis are carried out. A 12-bit non-binary SAR ADC with self-calibration is designed based on the TSMC 40nm CMOS process, which reduces the capacitance area, improves the conversion accuracy, and eliminates most of the errors caused by non-ideal factors. Simulation results show that the ADC's SNDR is 72.01dB, and INL within +1.2/-1LSB, meets most of the market requirements.

Keywords: SAR ADC; non-binary; self-calibration; capacitor array mismatch; comparator offset; intelligent sensing

1. INTRODUCTION

In recent years, with the rapid development of SoC in various fields, higher requirements have been put forward for the performance of CMOS analog-to-digital converters (ADCs) [1-3]. At present, the common ADC structures on the market include Flash ADC, Pipeline ADC, SAR ADC, and Sigma-Delta $\Sigma - \Delta$ ADC, and it can be seen from Table 1 that different structures bring different electrical characteristics. SAR ADC has the characteristics of medium conversion speed and accuracy, low power consumption and small area, and is widely used in various consumer products.

Table 1. Several common ADC electrical characteristics

Structure	Resolution	Speed	Power
Flash	<8 bit	fast	high
Pipeline	10~14bit	fast	medium
SAR	8~16bit	medium	low
Sigma-Delta	16~31bit	slow	medium

The digital-to-analog converters (DAC) in traditional SAR ADC are typically implemented with binary weighted capacitor arrays, but as the resolution increases, the capacitor array size increases proportionally, resulting in significant area and wasted power consumption. Therefore, segmented capacitive arrays are typically used in SAR ADCs above 10 bit to reduce capacitance area [2]. In the SAR ADC, due to the device mismatch caused by process deviation, the error generated at ADC quantization seriously limits it's performance. The error mainly include nonlinear errors caused by capacitor mismatch; comparator offset error due to mismatch between the MOS tubes.

In this paper, a 12-bit SAR ADC with self-calibration using a segmented non-binary capacitor array architecture is designed. Technology of capacitor calibration and offset cancellation correction are implemented in it, which can reduce errors caused by capacitor mismatch and comparator offset, improve the conversion accuracy of SAR ADC. Simulation using Cadence to build circuits shows that the ADC achieves the desired specifications.

2. CIRCUIT IMPLEMENT

2.1 ADC Circuit Structure

The proposed ADC structure is shown in Figure 2.1. It includes a pre-stage AFE, a main capacitor array DAC, a Bootstrap switch , a comparator, a sub-DAC for comparator offset calibration, and a SAR control logic controller. The proposed SAR ADC uses a nonbinary split capacitive array DAC consisting of a 6-bit binary weighted capacitor array and a 9-bit non-binary redundant capacitor array.

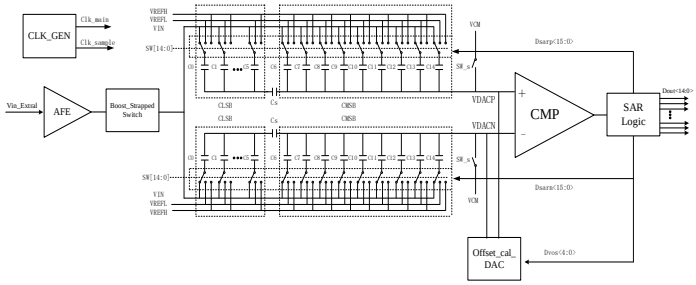

Figure. 2.1 Proposed Non-binary SAR ADC structure

The working process of this design is divided into two phases, the power-on self-calibration phase and the analog-to-digital conversion stage.The mismatch and offset are calibrated at the beginning of power up, and obtain the best capacitor weights [4]. After calibration, the final weights are updated in registers, and in normal conversion mode, the ADC conversion result is combined with the corresponding weight to convert 15-bit data to a 12-bit binary output. Compared with the traditional split binary SAR ADC, it only needs 196 unit capacitors, which greatly reduces the capacitor array size and reduces the power consumption of the capacitor array.

3.1.1 Sturcture of Non-binary Capacitor Array

The proposed weight of the non-binary capacitor array is shown in Figure 2.2. According to the sub-radix-2 (sub-binary) DAC capacitor array theory proposed by LIU W et al.

[5], it can be seen from Figure 2.2 that the weight values of the high-bit capacitors are less than the sum of the weight values of other low-bit capacitors, satisfying the sub-binary relationship, and the redundancy value of each capacitor is > 31LSB, about 3mV, which has good redundancy characteristics, so the high-bit comparison error can be corrected.

	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
Weight	1	2	4	8	16	32	33	66	99	165	264	363	594	924	1518
Sum	2	4	8	16	32	64	97	163	262	427	691	1054	1648	2572	4090
Redundancy	0	0	0	0	0	0	31	31	64	97	163	328	460	724	1054

Figure. 2.2 Non-binary capacitor array weight

2.2 Self-Calibration

2.2.1 Comparator offset cancellation

This design adopts digital front-end calibration scheme[6], before the SAR ADC power on, the SAR ADC calibrates the comparator offset firstly. After the calibration done, the capacitor mismatch calibration process is entered, and generates a flag signal when it done. Then the normal conversion starts when the sample clock comes, after convertion the 15bit output datas will be calculated according to the corresponding weight and aquire the final 12bit results. The details of self-calibration process is as follows.

Because comparator offset consumes redundancy of the capacitor array, this design calibrates the comparator offset firstly, after power up done [7]. In order to avoid errors caused by mismatch of main DAC, a comparator offset calibration sub-DAC is built, and the unit capacitance is taken by 1fF to reduce the size of the calibration capacitor. As shown in Figure 2.3, where Vip and Vin are connected to the positive and negative terminals of the comparator, respectively. At the beginning of the offset calibration, Vip and Vin are connected to the common-mode voltage Vcm. At the same time, the comparator input is disconnected from the main capacitor array, the capacitor lower plate is connected to ground, and the both capacitor arrays store the same charge. After that, the common mode is disconnected, and due to the presence of the comparator offset, an offset voltage Vos is superimposed on the Vip and Vin voltages, and the traditional dichotomy is used to complete the quantization of the comparator offset[8]. The quantization results are sent to the digital part, which obtains the multiple offset calibration codes by triggering the offset calibration multiple times, averaging them into registers, and passing them into the ADC in subsequent processes through the registers for offset elimination.

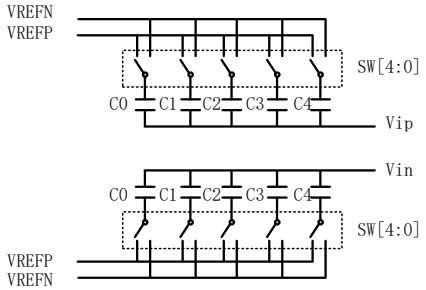

Figure. 2.3 Sub-DAC Capacitor Arrary

2.2.2 Capacitor array self-calibration process

The capacitor mismatch in low bit segment is small, so a binary capacitor array is used instead of calibrated. In the capacitance array self-calibration process, the upper 9-bit capacitor is calibrated. The 7th bit is calibrated firstly, in the sampling stage, the upper and lower plates of all capacitors are connected to Vcm, in the quantization stage, the lower plate of the high 8-bit capacitance is still connected to Vcm, the 7th bit is forced to Vref, the rest of the capacitance is normalized, and the quantization result Dout1 is obtained. Then the 7th bit capacitor is forcibly connected to Vss, and the remaining capacitors are normalized to obtain the quantization result Dout2. The two results are subtracted to get the 7th bit mismatch value, which is processed by a numerical algorithm, and the capacitance weight value of this bit is updated and recorded in the register. After the 7th bit capacitor calibration is completed, the 8~15th bit capacitor is calibrated in the same way, and in the normal conversion process, the output of each code is multiplied by the corresponding weight to obtain the 12bit digital output. The ADC output code processing principle is shown in Figure 2.4.

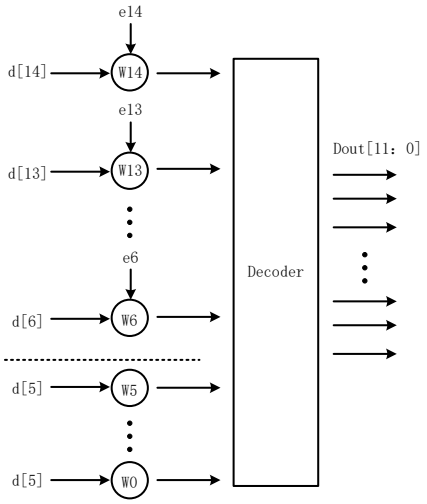

Figure. 2.4 Output principle of capacitor array calibration result

2.3 Convertion Process

After the power-up self-calibration is complete, the ADC begins normal analog-to-digital conversion work, which is divided into sampling and conversion stage. The proposed ADC uses synchronous timing logic, as shown in Figure 2.5. The clk_main is an external input master clock with a frequency of 20Mhz. clk_sample is an internal 1Mhz sample clock, generated by CLK_GEN circuit. clk_cmp is the comparator clock, according to the first-order RC network full response equation[9], as shown in Equation(1.1).

$$u(t) = u(\infty)\left(1 - e^{-\frac{t}{RC}}\right) \tag{1.1}$$

Even if the switch resistor R=20Ω, the capacitance C=5pF, the time constant is 100ps, and the half comparator clock cycle is much greater than 4RC, the DAC is guaranteed to fully settle. The sampled signal is converted analog-to-digital through 15 comparator clocks.

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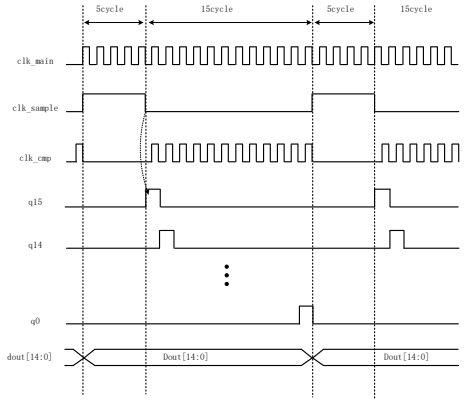

Figure. 2.5 Timing of this SAR ADC

2.3.1 Sampling

In order to reduce the influence of substrate noise on signal sampling, the lower plate sampling scheme is adopted in this design. When the clk_sample is high, the sampling stage is entered, and the SW_s switch is closed, and the capacitor C_{MSB} the upper plate of the high-bit segment are connected to the common-mode voltage V_{CM}. The positive capacitor array of the comparator C_{DACP}, the lower plate is connected to the input signal Vin, and the negative capacitor array C_{DACN} the lower plate of the comparator is connected to the reference low voltage V_{REFL}. At this time, the total amount of charge stored in the C_{DACP} and C_{DACN} capacitor arrays are:

$$Q_{DACP}=(V_{cm}-V_{in})\cdot C_{MSB,tot}+(V_{cm}-V_{in})\cdot C_{eq,L} \quad (1.2)$$

$$Q_{DACN}=(V_{cm}-V_{REFL})\cdot C_{MSB,tot}+(V_{cm}-V_{REFL})\cdot C_{eq,L} \quad (1.3)$$

$$C_{eq,L}=\frac{C_{LSB,tot}\cdot C_S}{C_{LSB,tot}+C_S} \quad (1.4)$$

where C_MSB,tot is the sum of all high-segment capacitances, and C_LSB,tot is the sum of the low-segment capacitance.

2.3.2 Convertion

After sampling, the clk_sample is pulled low, the upper plate of the capacitor array is disconnected from the common-mode voltage VCM, the comparator is working controled by clk_cmp, and the ADC enters the conversion process. During the conversion process, the capacitor array switch SW [14:0] is controlled by SAR logic outputs Dsarp [14:0] and Dsarn [14:0], so that the V_{DACP} voltage and the V_{DACN} voltage are approached successively to complete the 15-bit data conversion. In the MSB conversion process, the lower plate of the highest capacitance at the V_{DACP} end is first connected to V_{REFH}, and the lower plate of the remaining capacitance is connected to V_{REFL}. All capacitors at the V_{DACN} terminal are permanently connected to the V_{REFL} plate at all data conversion stages.

At this time, the charge stored in the V_{DACP} and V_{DACN} terminal capacitor arrays are:

$$Q_{DACP}=(V_{DACP}-V_{REFH})\cdot C_{MSB}+(V_{DACP}-V_{REFL})\cdot C_{M,R}+(V_{DACP}-V_{REFL})\cdot C_{eq,L} \quad (1.5)$$

$$Q_{DACN}=(V_{DACN}-V_{REFL})\cdot C_{MSB,tot}+(V_{cm}-V_{REFLO})\cdot C_{eq,L} \quad (1.6)$$

where $C_{M,R}=C_{MSB,tot}-C_{MSB}$, because there is no discharge path between the sampling and conversion stage, thus the V_{DACN} and V_{DACP} voltages are changed, and the two voltages are compared by the comparator to obtain the highest output, and the state of the switch SW [14:0] is controlled according to the output. And the next highest comparison is made when the next comparison clock comes.

3. SIMULATION RESULTES

According to the above structure, a 1Msps sampling speed 12bit SAR ADC is designed and realized based on the TSMC40nm process, and the circuit is simulated using the Cadence ADE, under the simulation conditions of IO voltage of 1.8V and external input clock of 40MHz.After 15 cycles of data conversion, the 15-bit data output is obtained to the digital part for weighting processing, and finally the 12-bit binary data output is obtained, and the voltage at both ends of the V_{DACP} and V_{DACN} is approached successively as shown in Figure 3.1.

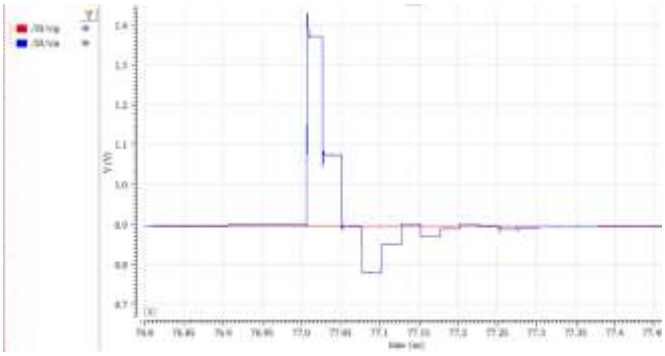

Figure. 3.1 Successive approximation simulation

Build a simulation circuit to simulate the dynamic performance of the ADC, under the simulation conditions of an input frequency of 414.06KHz and a sampling frequency of 1MHz, 4096 points are sampled, and 12-bit binary parallel data is obtained after conversion, and a fast Fourier transform is performed on the results, and the simulation results are shown in Figure 3.2.

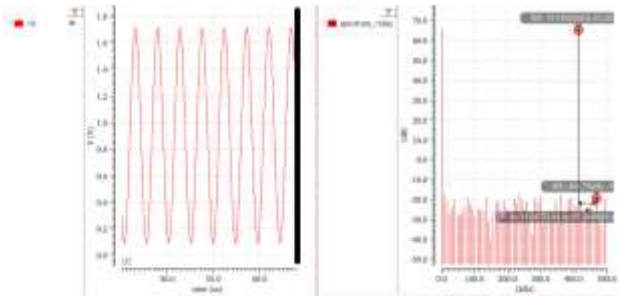

Figure. 3.2 Output wave FFT simulation result

The performance parameters of the 12-bit SAR ADC designed in this article are shown in Table 2.

Table 2. ADC Performance Summary

Parameter	Conditions	Result
ENOB	Fin=414.0625KHz Rin=10 KΩ VREF=1.8~3.3V	11.54bit
SNDR		72.01dB
THD		-83.24dB
SFDR		85.06dB

4. CONCLUSION

Based on the TSMC 40nm CMOS process, this paper designs a 12-bit SAR-ADC with self-calibration, optimizes the SAR-ADC structure, adopts a non-binary split capacitor array structure, reduces the capacitance area, and leaves sufficient redundant bits for calibration. In addition, a non-ideal factor calibration method is proposed to calibrate non-ideal factors such as comparator offset and capacitor array mismatch in the ADC, and at the same time, the non-ideal factors can be quantified and presented in the form of code, which can help designers accurately judge process errors and adjust the circuit. The simulation result shows the ENOB of this ADC reaches 11.54bit, the SNR is 72.01dB. The measured results show that the effective number of the ADC after calibration reaches 11.2bit, while compared with the ADC without calibration, the ENOB is 1~2bit higher, which has a high cost performance in the current consumer electronics field.

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