International Journal of Computer Applications Technology and Research
Volume 12–Issue 04, 01-04, 2023, ISSN:-2319–8656
DOI:10.7753/IJCATR1204.1001

Design of High-Speed SAR ADC based on 40nm CMOS Process

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Abstract: In this paper, a high-speed successive approximation analog-to-digital converter is designed based on a 40 nm CMOS process. A split-capacitor Vcm-Based switching strategy is designed, which is able to keep the output common-mode voltage constant for the DAC capacitor array without using Vcm level drive, while saving half of the capacitance compared to the conventional switching strategy and greatly reducing the area consumption. It also combines the features of binary redundancy technology and non-binary redundancy technology by splitting the highest bit capacitor to the lower bit, which enables the DAC array to generate two additional redundant bits without adding other capacitors, reducing its requirements for noise and establishment accuracy; and it adopts asynchronous timing control without external clocks, which is conducive to improving the speed of SAR ADCs and reducing the design complexity. The designed SAR ADC achieves 9.83 bit effective bits, 60.9 dB signal-to-noise distortion ratio, 77.2 dB spurious-free dynamic range, 1.68 mW overall power consumption, and 18.46 fJ/conv-step superiority at a supply voltage of 1.1 V and a sampling frequency of 100 MHz through simulation.
Keywords: high-speed digital-to-analog converter; redundant bits; capacitive splitting; asynchronous logic

1. INTRODUCTION

With the growing demand for ultra-low power systems on chip (SOC), which involve a large number of sensing with analog to digital signal conversion needs and need to be powered, such as mobile and Internet of Things (IOT), medical instruments and other devices. Low-power, low-area ADCs with medium resolution (8-16 bits) and speed (10-100 MS/s) are well suited for these applications, and advances in this type of ADC not only reduce power consumption and extend power cycles, but also provide significant space savings due to their small chip area. Among these common types of ADCs, SAR ADCs use a binary search algorithm, have a simple circuit structure, low power consumption, low requirements for analog circuits, high robustness, and are not process sensitive, which fits well with the trend of process size reduction.

The literature points out [1] that the current SAR ADC design faces many challenges. (1) Achieving a high linearity DAC array design [2], which is used to generate the internal reference voltage during conversion. (2) The maximum achievable number of effective bits is limited by the noise of the comparator [3]. (3) The signal-to-noise ratio of the ADC is limited by the front-end sampling circuit KT/C noise [4]. (4) Unstable supply voltages may lead to unstable reference voltages causing the circuit not to operate properly, especially in low-power SAR ADC designs [5]. There are some trade-offs in SAR ADC implementation, for example, some additional circuitry is essential to achieve low noise, but this may introduce additional area and energy consumption, and high robustness design has the same problem. For high-resolution designs of SAR ADCs, more comparison cycles are inevitable, which may lead to poor speed conditions or more severe energy consumption. Although trade-offs are important, it should be noted in the design that the specific design must be coordinated with the system design requirements and the trade-offs must serve the core metrics, so the core optimization metrics for SAR ADC design are currently focused on the following three points: low power consumption, high speed and high accuracy.

In this paper, a "capacitance splitting" Vcm-Based switching strategy for DAC arrays is designed based on the 40nm process, so that the DAC arrays can be switched without the need of Vcm level driving and the output common mode voltage can be maintained constant. At the same time, a non-binary capacitance reorganization method is adopted to add two extra redundant bits to the DAC capacitance array without increasing the total amount of capacitance, which increases the tolerance of SAR ADC to comparator noise and reduces the circuit requirement for DAC array setup time, thus realizing the high-speed SAR ADC design.

2. SAR ADC STRUCTURE DESIGN

As shown in Figure 1, the overall structure of the SAR ADC consists of five parts: sample-and-hold circuit, DAC array, comparator, SAR asynchronous logic, and digital error correction circuit. The DAC array adopts an all-capacitor structure and adds two extra redundant capacitors by non-binary capacitor reorganization, which reduces the requirement of establishing accuracy of DAC capacitor array. The switching strategy of the DAC array uses a Vcm-Based switching strategy combined with a "capacitor splitting" technique to keep the output common-mode level constant without the need for Vcm-Based levels. The main function of SAR asynchronous logic is to generate the high-frequency clock inside the SAR ADC and output the digital code word of the comparator comparison result, and to generate the control signal of the switch in the DAC array according to the comparison result. The digital error correction circuit is to convert the 12-bit digital code word output from the SAR asynchronous logic into a 10-bit binary number and output it.

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The sampling clock in the figure is an externally provided clock with a frequency of 100MHz and a duty cycle of 20%, which means that during the whole system operation, the sampling time is 2ns and the conversion cycle is 8ns, and because two redundant bits are added, the conversion cycle is divided into 12 comparison cycles. The working process is as follows: when the sampling clock is high, the SAR ADC is in the sampling stage, and the input signal is sampled through the sampling circuit to capture the signal into the DAC capacitor array. When the sampling clock is low, the SAR ADC is in the conversion stage and the comparator starts to compare the sampled input signal and transmits the result to the SAR logic, which outputs the comparison result and generates a control signal to control the DAC array, and the DAC array generates a new voltage input comparator until the end of 12 comparison cycles, and finally the digital error correction circuit converts the 12-bit digital code word The final digital error correction circuit converts the 12-bit digital code word into a 10-bit binary number and outputs it.

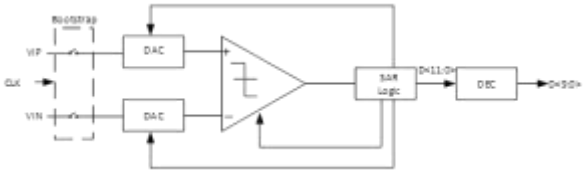

Figure 1. SAR Structure Diagram

3. CIRCUIT STRUCTURE DESIGN

3.1 Bootstrap Circuits

Figure 2 shows the gate voltage bootstrap switching circuit in this design. From the figure, CLK is the clock provided externally, and CLKB and CLK are opposite clocks. In the hold phase, CLK is low, node D is high, M5 tube is off, at this time CLKB is high, so that M3 is on, node A is pulled down to ground, while M8 is also on, passing the low level to node G. M4 is on so that node B is charged to VDD, at this time the upper end of capacitor C1 is connected to VDD, the lower end is grounded, and sampling switch M9 is off. In the sampling stage, CLKB is low, M8 is off, and M3 is also off, CLK is high, M2 conducts node D also from high level discharge to low level, so that M5 conducts, at this time, node B and node G are connected, so M7 conducts, node A changes from low level to Vin, because there is no discharge loop, so the charge at both ends of capacitor C1 is conserved, and the voltage of node G is raised to VDD+Vin At this time, the Vgs of sampling tube M9 remains unchanged, so its conduction resistance does not change with the change of voltage. It should be noted that the substrate of M4 tube needs to be shorted with node B. If M4 is connected to VDD according to the conventional connection, M4 is PMOS, and PMOS is generally made in n-well in the layout, there is a forward diode from node B to VDD, so that the voltage at point B can only reach VDD+0.7V at the highest, and when there is no secondary tube, it can reach 2VDD, which will seriously limit the swing..

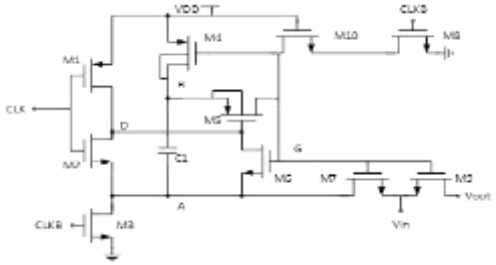

Figure 2. Bootstrap Switch Circuit Diagram

3.2 DAC Array

In this design, the Vcm-Based switching strategy is based on splitting the capacitor, which is difficult to provide Vcm in a low-voltage process. The capacitance of each bit is divided into two equal parts, one part of the lower pole plate is connected to Vcm and the other part is connected to ground. The capacitor connected to Vref is the high level capacitor, and the one connected to ground is the low level capacitor. Since the size of Vcm is half of VDD, the charge stored in the total capacitor is the same after the "capacitor splitting" technique. Meanwhile, the non-binary capacitance reorganization method is used to achieve a certain amount of redundancy by splitting the high level capacitance and assigning it to the low level capacitance. This method does not need to add additional redundant bit capacitors compared to binary redundancy, which greatly saves area, and the base of the weight is no longer 2, but smaller than 2, which can bring a certain amount of fault tolerance to the ADC when an establishment error occurs. The switching method is shown in Figure 3. The design is a 10bit SAR ADC, which introduces two redundant bits, and its MSB capacitance weight is 512, of which 64 capacitors are now split and assigned to the lower capacitor, and in the previous design, due to the "capacitance splitting technique", the lower capacitor is assigned to ensure that In the previous design, due to the "capacitance splitting technique", the lower capacitors are assigned to the even number of the corresponding bits of the DAC capacitor array.

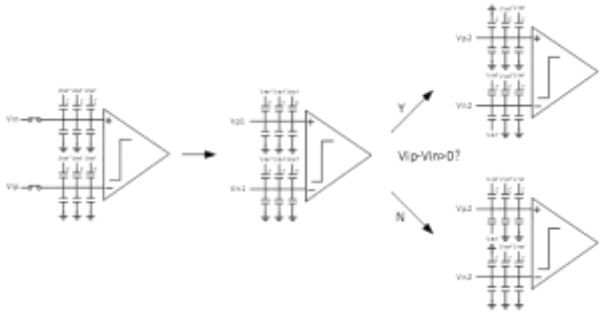

Figure 3. Vcm-Based Switching Based on Split Capacitor

3.3 SAR Logic

The entire SAR ADC asynchronous timing basic logic circuit is shown in Figure 4, where SOC is the sample clock simple inverse generation, used to control the on and off of the asynchronous loop, VALD is used to indicate the working state of the comparator, when the comparator completes the comparison of one bit, VALD = 1. CLKC is the asynchronous SAR ADC internal self-generated high-speed clock, used to control the working state of the comparator. When CLKC=0, the comparator is reset, and when CLKC=1, the comparator compares the comparator. CLKi is the data acquisition clock, which is used to control the acquisition of comparator output results and switches in the DAC array. OVER is the output signal after the last 12 comparisons are completed.

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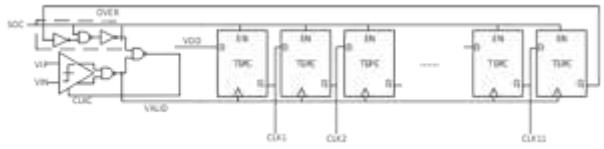

Figure 4. SAR ADC Asynchronous Timing Logic

3.4 Digital Error Correction

Since two redundancies are added to the DAC capacitor array, the total number of bits becomes 12, so the digital error correction（DEC） module is now needed to convert the 12-bit digital code word into a 10-bit binary number output. Since the method of non-binary capacitor reorganization is used, in splitting the MSB capacitors are disassembled with a power of two put, and the weight of each bit is known above, so the weight of each bit can be expressed in a power-of-two summation, and the conversion process can be represented in Figure 5.

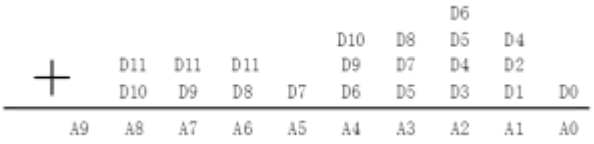

Figure 5. Conversion process

4. SIMULATION RESUITS AND ANALYSIS

The entire 10bit 100Ms/s SAR ADC has been built by verifying the feasibility of each of the above modules. In order to verify whether its overall performance meets the design specifications, a signal with close to full swing is input with a frequency of about 7.52MHz at a supply voltage of 1.1V, a temperature of 25°C, a clock frequency of 100MHz under TT model and a duty cycle of 20%, and the output code word is output through the ideal DAC to obtain the output waveform after sampling and conversion. The output waveform is exported to Cadence simulation software in CSV file format, imported to MATLAB for simulation, and 1024 points are taken for FFT analysis, and the final result is shown in Figure 6.

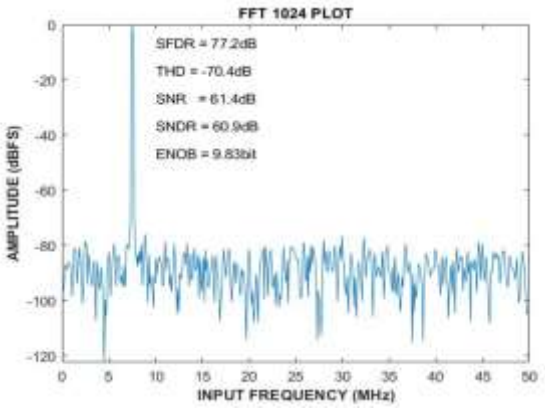

Figure 6. Conversion process

The performance of the final SAR ADC designed in this thesis is shown in Table 1.

Table 1. SAR ADC performance parameters

Design Parameters	Performance Indicators
Supply Voltage	1.1V
Resulotion	10bit
Sampling Rate	100Ms/s
ENOB	9.83bit
SFDR	77.2dB
SNDR	60.9dB
Power	1.68mW
FOM	18.46 fJ/conv-step

In order to design the reliability of the SAR ADC under different environments, the dynamic performance and power consumption under two process angles of ff and ss were simulated at 80°C and -20°C, respectively, as shown in Table 2.

Table 2. Simulation of performance at different corner

	ff -20℃	**ff 80℃**	**ss -20℃**	**ss 80℃**
ENOB(bit)	9.869	9.820	9.841	9.873
SFDR(dB)	77.53	77.91	77.7	78.3
SNDR(dB)	61.17	60.88	61.01	61.2
Power（mV）	1.703	2.369	1.617	1.681

Table 3 compares the performance of the SAR ADC designed in this thesis with that of 10-bit precision SAR ADCs designed in other literature.

Table 3. Simulation of performance at different corner

	[7]	**[8]**	**This work**
Process	65nm	20nm	40nm
ENOB	9.51 bit	9.19 bit	9.83 bit
Sampling Rate	100 Ms/s	320 Ms/s	100 Ms/s
Power	1.13 mV	1.52 mV	1.68 mV

5. CONCLUSIONS

In this paper, we design a 10-bit 100MS/s high-speed asynchronous SAR ADC in 40nm process, analyze the energy consumption of different switching strategies, and combine the "capacitance splitting" technology to design a Vcm-based switching strategy based on "capacitance splitting". Based switching strategy of DAC array is designed, so that the DAC array can be switched without Vcm level drive and the output common-mode voltage can be maintained constant. At the same time, the non-binary capacitor reorganization method is adopted to add two extra redundant bits to the DAC capacitor array without increasing the total amount of capacitors, which increases the tolerance of the SAR ADC to the comparator noise and reduces the circuit's requirement for the DAC array build-up time, and improves the speed of the SAR ADC to a certain extent. Completed the overall circuit building of SAR logic and realized the asynchronous timing control of SAR ADC. Completed the construction of the digital error correction circuit module and realized the conversion of 12-bit redundant output codes to 10-bit binary numbers. Simulation verification and layout design of the overall circuit were performed at different process angles. The simulation obtained an effective bit count of 9.83 bits, a spurious-free dynamic range of 77.2 dB, a signal-to-noise distortion ratio of 60.9 dB, and a power consumption of 1.68 mW in a 40 nm

process with a 1.1 V supply voltage. the final optimal value is 18.46 fJ/conv-step.

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