International Journal of Computer Applications Technology and Research
Volume 12–Issue 04, 23-26, 2023, ISSN:-2319–8656
DOI:10.7753/IJCATR1204.1006

Design of a 14-bit Pipelined ADC using Ring Amplifier

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Abstract: With the progress of integrated circuit technology, the intrinsic gain of transistors has become increasingly low, and the power consumption and complexity of OTA operational amplifiers have become higher, increasing the overall design difficulty of pipeline ADC. In order to improve the gain of the operational amplifier, improve the overall accuracy of the ADC, and reduce circuit power consumption, a 14-bit 20MSPS analog-to-digital converter with a pipeline structure of 2.5bit-2.5bit-2.5bit-2.5bit-2.5bit-2.5bit-2.5bit-2.5bit-2bit was designed using the SMIC 40nm process and analog drive digital technology under a 1.2V power supply voltage based on a new type of ring amplifier.The simulation results show that the SNDR of the input low-frequency signal pipeline ADC is 70.47dB, the SFDR is 85.5dB, and the ENOB is 11.45bit. When inputting high-frequency signals, the SNDR of the pipeline ADC is 68.35dB, the SFDR is 81.3dB, and the ENOB is 11.07bit.

Keywords: Ring amplifier; OTA, pipeline ADC; AP-CMOS; fully differential; MDAC

1. INTRODUCTION

Currently, most pipeline ADC structures use traditional operational transconductance amplifiers (OTAs) or open loop amplifiers as interstage operational amplifiers, and the power consumption in pipeline ADC mainly comes from the operational amplifiers in each stage of MDAC[1]. Operational amplifiers in MDAC generally require very high gain to ensure transmission accuracy. With the progress of integrated circuit technology, the intrinsic gain of transistors has become increasingly low. In order to ensure the high gain of operational amplifiers, the use of gain bootstrapping, digital calibration, and other technologies have made the power consumption and complexity of circuits higher, and increased the overall design difficulty of ADCs. In order to improve the gain of operational amplifiers, improve the overall accuracy of ADC, and reduce circuit power consumption, the industry has been looking for a new type of operational amplifier that can replace traditional OTAs for pipeline ADC structures.

Table 1. Comparison of Common Operational Amplifiers

Amplifier type	Gain	Power	Linearity
Traditional OTA	limited	high	secondary
Open loop amplifier	secondary	secondary	low
Dynamic amplifier	high	very low	low
Ring amplifier	very high	low	high

With the power supply voltage is 1.2V, using traditional Cassode high-gain OTA as an operational amplifier will result in insufficient voltage redundancy. In order to ensure low power consumption while reducing the use of gain enhancement techniques, the gain of OTA will also be greatly limited. In order to avoid the problems of insufficient gain and high power consumption caused by traditional operational amplifiers, academic circles have also proposed solutions such as open-loop amplifiers[2], dynamic amplifiers[3], and ring amplifiers. A comparison of commonly used operational amplifiers is shown in Table 1. In practical design, open loop amplifier structures have PVT performance issues, and calibration techniques are often needed to ensure their gain. Dynamic amplifiers have fast amplification speed and low power consumption due to their switch controlled operation. However, due to their open loop structure, their accuracy and linearity are relatively low.

Ring Amplifier was first proposed and applied to pipeline ADC in 2012[4]. It has very high gain and rail to rail output swing, and its power consumption is very low. It meets the requirements of pipeline ADC for high gain and low power consumption of operational amplifiers, perfectly replacing traditional OTA operational amplifiers, and meets the overall design requirements of pipeline ADC.

In this paper, based on the SMIC 40nm process in SMIC International, a 14-bit 20MSPS high-precision analog-to-digital converter with a pipeline architecture of 2.5bit-2.5bit-2.5bit-2.5bit-2.5bit-2.5bit-2bit is designed using a ring amplifier at a 1.2V power supply voltage.The simulation results of the circuit built by Cadence show that the ADC meets the required indicators.

2. CIRCUIT IMPLEMENT

2.1 ADC Circuit Structure

The 14 bit 20 MSPS pipeline ADC designed in this article adopts a pipeline structure after considering redundancy bits. The sub level structure is shown in Figure 2.1. The pipeline ADC is mainly composed of six sub conversion stages and one level Flash-ADC, digital circuits, and clock circuits. Sub-ADC adopts Flash-ADC structure. MDAC (Gain Digital to Analog Conversion Unit): A new ring amplifier structure is used to perform digital to analog conversion of sub ADC outputs and amplify residual signals.

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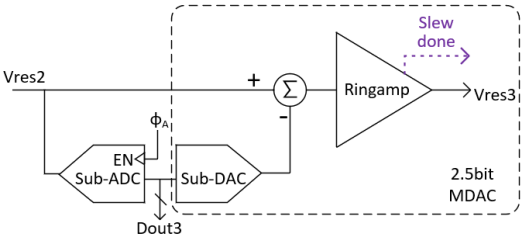

Figure. 2.1 The sub level structure of pipeline ADC

Each stage of the pipeline ADC consists of Sub-ADC, Sub-DAC, and subtraction operational amplifier circuits, wherein the MDAC consists of a switched capacitor circuit and an operational amplifier. The slew done signal generated by the dead band voltage of a fully differential ring amplifier is used to convert the input analog signal into an output that is close to a digital signal. The generated signal is used to start the next level ADC circuit, reducing the impact of clock jitter signals on each level of the waterline circuit, and improving the signal to noise ratio of the ADC.

2.2 Ring amplifier

2.2.1 Ring oscillator structure

The structure of a ring amplifier is derived from a ring oscillator, which has a similar circuit structure to that of a ring oscillator. A ring oscillator composed of a three-level CMOS inverter is shown in Figure 2.2.

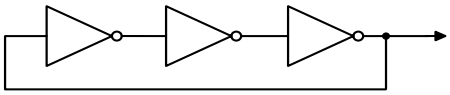

Figure. 2.2 Ring oscillator structure

The amplification function of a ring amplifier is modified based on a ring oscillator, which is created by dividing the oscillator into two signal paths and embedding different offsets in each path[5].When placed in switched capacitor feedback, a set of internal mechanisms generates stability and allows the oscillator to act as an amplifier.

2.2.2 Switched capacitor ring amplifier

Although the basic structure of a ring amplifier is simple, its operating principle is relatively complex. The traditional switched capacitor ring amplifier model is shown in Figure 2.3, when the loop amplifier is placed in a switched capacitor feedback structure and the dead band voltage V_{DZ} is equal to 0V, the loop amplifier is functionally identical to a three-level inverter loop oscillator.

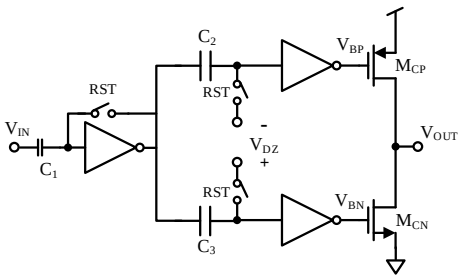

Figure. 2.3 Switched capacitor ring amplifier structure

When the deadzone voltage increases, the output waveform is stably formed at the intersection of the deadzone, and both the tubes M_{CN} and M_{CP} are closed. At this point, the effective gain through the oscillator is zero, so the average gain and oscillation frequency decrease. Under certain critical dead band sizes, this effect reduces the unit gain bandwidth of the oscillator below the frequency corresponding to a 180 ° phase delay. When the deadzone is set large enough to produce stable settling, a ring amplifier is used as an amplifier, which is particularly suitable for working in small size, low voltage environments, is not affected by power supply voltage drops, and can be amplified with rail to rail output swing.

2.2.3 Fully differential ring amplifier

In order to fully utilize the high gain characteristics of a ring amplifier while addressing the limitations of a single ended structure, Figure 2.4 presents a fully differential ring amplifier.In order to make the ring amplifier fully differential, we replaced the first stage of two self biased ring amplifiers with a single differential pair[6].Based on an ordinary fully differential ring amplifier, a novel fully differential ring amplifier using a reverse parallel structure and adding a clock generation and control circuit is proposed.

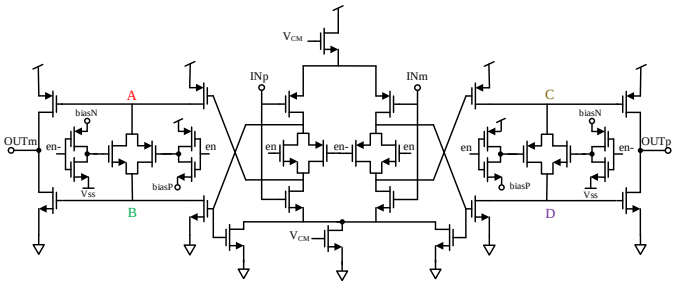

Figure. 2.4 Fully differential ring amplifier structure

The improved fully differential ring amplifier is based on a resistor self biasing differential structure, with the deadzone voltage control circuit changed from a resistor to an AP-CMOS structure[7].An en control terminal is added to the gate of the AP-CMOS, making it an adjustable CMOS control terminal between nodes A, B, C, and D. In the off state (en=0), these CMOS structures act as open switches, and the circuit is closed. In the open state (en=1), the circuit is of a working AP-CMOS ring amplifier structure. The CMOS structure operating in a floating battery state increases the maximum overdrive voltage of the device, reducing the size required for the circuit, thereby reducing parasitic effects within the ring amplifier, and improving the speed and efficiency of the overall ring amplifier.When using a smaller process size of 40 nm, the parasitic effects inside the ring amplifier will be significantly reduced. The size of each stage of the ring amplifier transistor is different, and the size of the first stage inverter A1 needs to be set large enough to increase the non dominant pole frequency. The transistor sizes for each stage from A1 to A3 are sequentially reduced to ensure sufficient phase margin for the ring amplifier.The transistor sizes of each amplifier stage of a fully differential ring amplifier are shown in Table 1.

Table 2. Device parameters of ring amplifier

RAMP	NLength	NWidth	PLength	PWidth
A1	40nm	1um	40nm	3.5um
A2	40nm	1um	40nm	3um
A3	500nm	200nm	500nm	900nm

2.3 MDAC circuit

2.3.1 Capacitance flip MDAC

The function of MDAC is to subtract the input signal from the result obtained by Sub-ADC, then multiply the difference to

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obtain the residual signal of the ADC at the current level, and then transmit the signal to the input terminal of the next level.Figure 2.5 shows the structure diagram of a 1.5bit capacitor flip type MDAC[8].

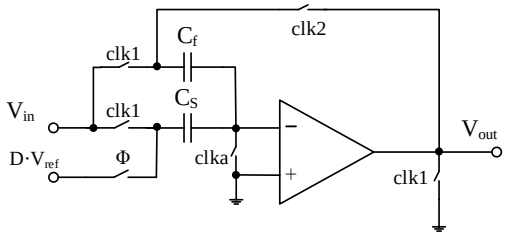

Figure. 2.5 1.5bit capacitor flip type MDAC

For capacitive flip over type MDAC, the capacitance C_s serves as both a sampling capacitor and a feedback capacitor, which is a loop feedback capacitor. The total sampling capacitance is $C_s + C_f$, and its feedback coefficient is:

$$\beta = \frac{C_f}{C_s+C_f} \tag{1.1}$$

During the operation of the MDAC circuit, both the sampling phase and the holding amplification phase capacitances satisfy the charge conservation principle. At this time, the operational amplifier gain is and ignores the finite gain and parasitic capacitance effects. The transfer function of the capacitance flip type MDAC is:

$$V_{out} = \frac{A}{1+A\beta}\left(V_{in} - D_i \cdot V_{ref}\frac{C_s}{C_s+C_f}\right) \tag{1.2}$$

2.3.2 Overall structure of MDAC

The 14-bit pipelined ADC in this article adopts a capacitance flip type 2.5bit per stage MDAC structure, which reduces the impact of non ideal factors and reduces the difficulty of amplifier design. The overall circuit structure of the MDAC is shown in Figure 2.5.

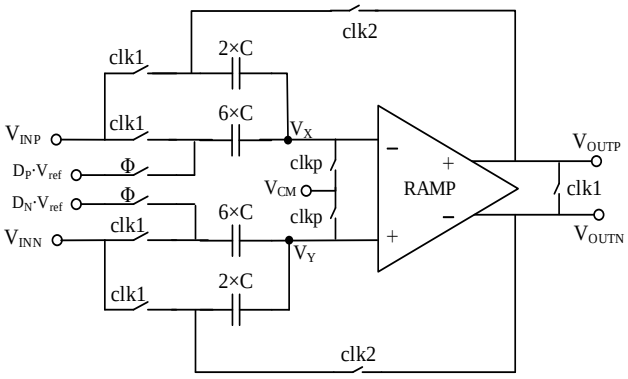

Figure. 2.6 Overall structure of MDAC circuit

Due to the 2.5bit redundant bit design of the MDAC, its interstage gain is 4.The MDAC composed of a fully differential structure has six sampling capacitors and two feedback capacitors on each side. It operates in the sampling and holding amplification phases using a bidirectional non overlapping clock, and its operating principle is similar to that of a 1.5bit capacitor flip type MDAC.The entire capacitance of the MDAC circuit during operation satisfies the law of charge conservation.The charge transfer equations for the input nodes X and Y of the operational amplifier during the sampling phase are as follows:

$$Q_X = (V_{CM} - V_{INP}) \cdot 8C \tag{1.3}$$

$$Q_Y = (V_{CM} - V_{INN}) \cdot 8C \tag{1.4}$$

Assuming that the number of 1 in each input digital code is n while maintaining the amplification phase, the charge transfer equations for nodes X and Y are as follows:

$$Q_X = (V_X - V_{REFP}) \cdot nC + (V_X - V_{REFN}) \cdot (6-n)C + (V_A - V_{OUTP}) \cdot 2C \tag{1.5}$$

$$Q_Y = (V_Y - V_{REFN}) \cdot nC + (V_Y - V_{REFP}) \cdot (6-n)C + (V_Y - V_{OUTN}) \cdot 2C \tag{1.6}$$

Without considering the parasitic capacitance at the input of the operational amplifier, the charge transfer equation for the sampling phase and the holding amplification phase is derived from the charge conservation law, and the 2.5-bit capacitance flip type MDAC transfer function is:

$$V_{OUT} = \frac{A}{A+4} \cdot 4\left(V_{IN} - \frac{n-3}{4}V_{REF}\right) \tag{1.7}$$

In the actual MDAC design, it is necessary to consider the limited gain and input parasitic capacitance of the operational amplifier, and the actual feedback coefficient of the MDAC will become smaller. Using a high-performance ring amplifier can improve the overall accuracy of the ADC.

3. SIMULATION RESULTES

Perform stability simulation on the ring amplifier, and the simulation results are shown in Figure 3.1. From the figure, it can be concluded that the low frequency gain of the operational amplifier is about 86.79 dB, and the unit gain bandwidth is about 670 MHz. At this time, the phase margin is about 62 deg, which meets the design requirements of the operational amplifier in MDAC.

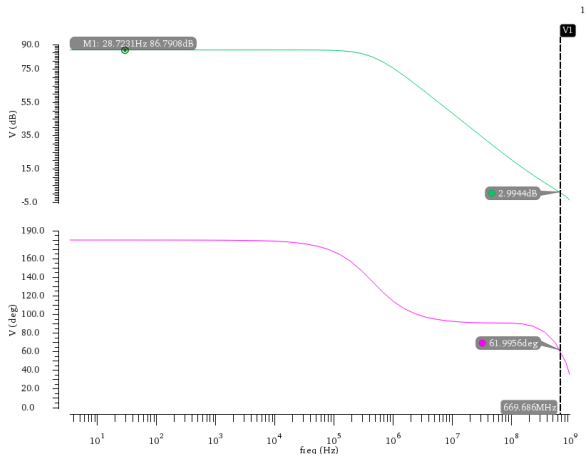

Figure. 3.1 Stability Simulation of Ring Amplifier

FFT analysis of ADC output data can obtain the spectrum characteristics of ADC, and then calculate various dynamic indicators.The simulation results of ADC dynamic performance are shown in Figure 3.2 and Figure 3.3.

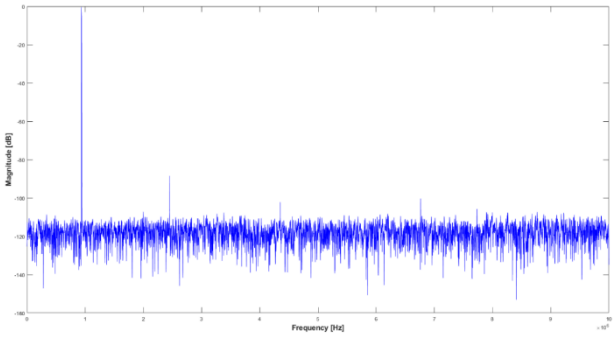

Figure. 3.2 Low frequency signal FFT simulation results

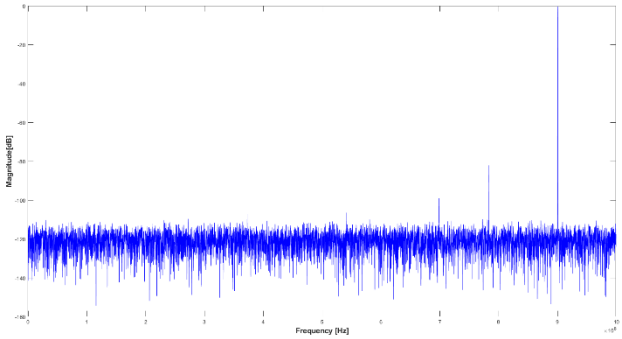

Figure. 3.3 High frequency signal FFT simulation results

The input signal frequency is 0.902099 MHz, the SNDR of the pipeline ADC is 70.47 dB, the SFDR is 85.5 dB, and the effective bit ENOB reaches 11.45 bits. The input signal frequency is 9.024658 MHz, the SNDR of the pipeline ADC is 68.35 dB, the SFDR is 81.3 dB, and the effective bit ENOB is 11.07 bit.

4. CONCLUSION

Based on the SMIC 40nm process, a 14-bit pipelined ADC with a sampling rate of 20 MSPS is designed and implemented under a 1.2V power supply voltage. A new type of ring amplifier is used, which can generate a slow done signal through an AP-CMOS structure. This solves the problem of high power consumption in traditional OTAs, reduces clock jitter, and improves the gain and bandwidth of operational amplifiers in the ADC.The simulation results show that when the input signal frequency is 0.902099 MHz, the SNDR of the pipeline ADC is 70.47 dB, the SFDR is 85.5 dB, and the effective bit ENOB reaches 11.45 bits. When the input signal frequency is 9.024658 MHz, the SNDR of the pipeline ADC is 68.35 dB, the SFDR is 81.3 dB, and the effective bit ENOB is 11.07 bit.

5. REFERENCES

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