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Design of Bit Width Converter Based on PCIE4.0

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Abstract: Aiming at the data bit width conversion module used in PCIE4.0 physical coding layer, this paper designs a backwards compatibility-capable implementation method, which combines the version below backwards compatibility 4.0. According to the data bit width selection signal BusWidth of MAC layer in PCIE protocol, the current running speed of PCIE is selected. So as to select the form of bit width conversion. The designed PCIE internal strobe signal is 32 bits wide, and the correctness of its coding operation mode is verified by using the description language of Verilog hardware and the joint simulation form of Verdi and VCS.

Keywords: compatibility; Bit width selection; High speed interface; PCIE4.0;

1. INTRODUCTION

PCI Express(PCIE) was originally designed as a local bus interconnection technology to connect CPU, GPU and I/O devices inside the machine, and has developed into a mature switching network, which is characterized by point-to-point end-to-end. Bus is a bridge connecting the interfaces between computer subsystems, and the interfaces between each subsystem are connected with each other through bus[1]. In the era of information technology explosion, people's demand for information transmission and data processing is increasing day by day. Compaq company puts forward the concept of distinguishing the system bus from I/O interface bus[2], which makes the high-speed processor develop rapidly. Compared with bus, the development of I/O bus is relatively slow, which makes I/O bus gradually become a major bottleneck in computer development. With the improvement of technology, PCIE has gradually moved towards a broader stage. PCIE is the most widely used industry standard for connecting hardware peripherals to computer systems. It uses point-to-point links, one of which contains 1 to 16 channels, and each channel is a full-duplex serial connection. In 1991[3], Intel Company proposed that when the bit width is expanded to 32 bits, its bandwidth can reach 133MB/s, and the data of this bus can be read and written suddenly, and the peripheral components of the supporting device can work in multiple groups at the same time[4]. PCIE4.0, the speed has been increased from 8Gbps to 16Gbps. In the PCIE version, the encoding form adopted for Gen1/Gen2 is 8b/10bde, but in Gen3/Gen4, it is 128b/130b. When developing to a high version protocol, the bit width of data changes with the setting of internal channels. This paper will design a bit width conversion module that can change the designed bit width only by modifying the code of the bit width conversion module.

2. DATA BIT WIDTH CONVERSION

The sending part of PCIE mainly converts the parallel data bit width transmitted by the MAC layer. The inner part width is defined as 32 bits, and the control signal of PCIE4.0 data is processed synchronously[5]. In this case, the processing of bit width is different due to the selection of BusWidth of bitwidth signal. When the selected bit width signal is in PCIE Gen1/Gen2, the encoding mode of the data is 8b/10b, and the input data bit width of this part can be selected as 8, 16 and 32[6]. However, the set data bit width channel is 32 bit width, so there are three ways to adjust the data bit width. When the data is in Gen3/Gen4, at this time the encoding mode of data processing is 128b/130b at this time the internal selection of the data communication number is still set to 32 bits wide, but at this time the expenditure of data input only 16, 32 two, so there are two ways to adjust the data. Therefore, according to the above data bit width selection, different bit width selection processing will be carried out[7].

3. DESIGN AND IMPLEMENTATION

Data bit width conversion mainly synchronizes the input data at the same bit width and rate during PCIE Gen3/Gen4. This data bit width conversion is mainly used to synchronize the input data with different bit width and rate under Gen3.0 and Gen4.0 protocols[8].

The design essence of data bit width conversion is signal processing under asynchronous clock. The TxstartBlock signal and the Tx_DataValid signal in the sys_clk clock domain need to be converted to the pclk clock domain according to the current rate requirement. The internal channel bit width is defined as 32 bits in the following three cases:

1. When the BUS_WIDTH signal is 00, the width of the data bit in the sys_clk clock field is the same as the width of the data bit inside the sys_clk clock field. The input signal only needs to be beaten and synchronized.

2. When the BUS_WIDTH signal is 01, the data bit width under sys_clk clock field is 16 bits, which is different from the internal data bit width, and the two clocks are different. Under PCle4.0, sys_clk is 1Ghz and pclk is 500Mhz, which is single-ratio fast to slow cross-clock domain processing. In order to prevent data leakage, level extension (handshake) is adopted.

3. When the BUS_Width signal is 10, the data bit width of sys_clk clock domain is 8 bits, which is different from the internal data bit width, and the two clocks are also different. Under PCle4.0, sys_clk is 2Ghz and pclk is 500Mhz. Level extension (handshake) is used to prevent leakage.

For data signals, as specified by the protocol, TxstartBlock signal will be extended by one beat and Tx_DataValid signal will be set low when the synchronization head of the transmitted data reaches the data bit width of the internal channel. If the signal Bus_Width is selected for different bit widths, the signal should be synchronized simultaneously. Table 1-1 lists the preceding signals.

Table 1-1 lists the involved input signals

Name	I/O	Description
sys_clk	I	MAC layer clock
sclk_rst_n	I	sys_clk clock reset signal, low reset
pclk	I	Internal data channel parallel clock
tx_DataValid	I	The Mac layer tells Phy that data transfer is valid and ignores data for a period when it is low
txstartBlock	I	Block start flag signal (for PCIe3.0/4.0)
BusWidth[1:0]	I	MAC layer data bit width is selected 00 : 32 01 : 16 10 : 8 11 : reserved
ss_mode_sync	O	Output data valid
data_2ififo	O	Output synchronous parallel data
TxstartBlock_ mac	O	Output the block start signal after the clock domain transition
Tx_DataValid _mac	O	Output data valid signal after clock domain conversion

4. SIMULATION ANALYSIS

Under the Gen3/Gen4 protocol, the input data with different bit widths and rates are synchronized. Figure 1-2 shows that when the data bit width selection signal BUS_WIDTH is 00, the bit width in the sys_clk clock domain is the same as the set bit width of the internal channel, and the synchronous beat output is performed.

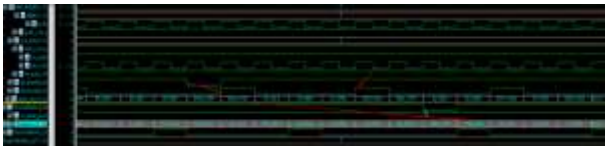

Figure 1-2 32-bit to 32-bit conversion

Figure 1-3 shows the data bit width conversion when the data bit width selection signal BUS_WIDTH is 01. At this time, it is the conversion from 16-bit to 32-bit width. At this time, the data of every two beats are combined into 32-bit data for output.

Figure 1-3 16-to 32-bit wide conversion

Figure 1-4 shows the data bit width conversion when the data bit width selection signal BUS_WIDTH is 10. At this time, the bit width of data is converted from 8 bits to 32 bits, and the data obtained every 4 beats are combined into 32-bit data for output.

Figure 1-4 8 to 32 bit width selection

5. CONCLUSION

By adjusting the bit width between data conversion modules, it can be obtained that under different PCIE versions, the running speed and bit width selection of PCIE can be judged according to the bit width selection signal. In order to facilitate the subsequent adjustment of PCIE bit width, we can increase its bit width selection. When the data bit width is 32 bits, its clock frequency is 500MHz, and the internal channel of its bit width selection is expanded to 64 bits. At this time, the clock frequency required by PCIE will not be 500MHz but 250MHz. With the design of the module bit width above, it can be explained that the desired data channel bit width can be achieved by adjusting the data bit width.

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