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Design and Implementation of Refresh and Timing Controller Unit for LPDDR2 Memory Controller

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Abstract: this paper presents a "Implementation of "Refresh And Timing Controller" unit for low power double data rate 2 memory controller (LPDDR2 MEMORY CONTROLLER). "Refresh and Timing Controller" unit plays a vital role for LPDDR2 memory controller .It maintains different timing parameters to handle various commands for memory like refresh, read and write operations and also performs Memory Initialization. Since it is low power DDR2 the maximum duration in power-down mode and deep power down mode is maintained by "Refresh and Timing Controller" unit. The refresh rate period is programmable using the Refresh Period Register. It supports "All Bank Refresh". The unit has timers to accommodate Refresh, Read/Write, and Power down modes. The RTL is done using the System Verilog. The design is simulated

Keywords: LPDDR2 MC; Design; Device initialization**;** Refresh requirement;Timing parameters

1. INTRODUCTION

Embedded systems usually have a limited amount of memory available; this is because of cost, size, power, weight or other constraints imposed by the overall system requirements. It may be necessary to control how this memory is allocated so that it can be used effectively. Handheld device like mobile, tablet etc are battery operated. For long time battery lasting better power optimization is required in those devices. Nowadays the devices are having multiple masters and share common memory for their applications. LPDDR2 is better fit for these kinds of devices. LPDDR2 memories consume low power. LPDDR2 memory controller accepts write/read commands from multiple masters and generates memory related commands. Functions of memory controller are

- solves different bandwidth requirement issues
- handles the "refresh" cycle for Memory.
- handles read and write operations with bank/row/column addressing.

Since these memories are made with capacitors, charge will leak continuously so refreshing is required memory controller will generate refresh commands as specified in JEDEC specification. For each refresh in a LPDDR2 row, the stored information in each cell is read out and then written back to itself as each LPDDR2 bit read is self-destructive. The refresh process is inevitable for maintaining data correctness, unfortunately, at the expense of power and bandwidth overhead.

This paper is organized as follows. The brief introduction to **"Refresh And Timing Controller"** "is given in section 2 describes top module of**" Refresh And Timing Controller"**, section 3 describes the implementation of **"Refresh And Timing Controller"** for LPDDR2 memory controller. Section 4 describes the result and analysis.

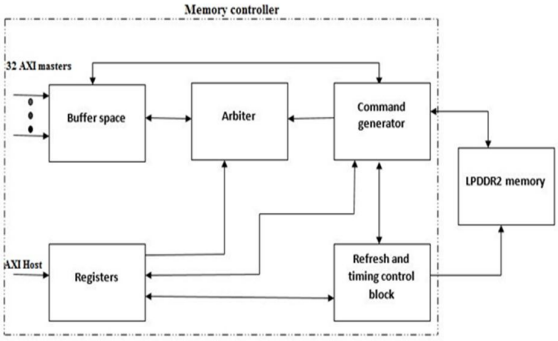

Figure 1: LPDDR2 Memory controller

See figure 1 the LPDDR2 memory controller,LPDDR2 MC's are used to drive DDR2 SDRAM, where data is transferred on the rising and falling access of the memory clock of the system without increasing the clock rate or increasing the bus width to the memory cell. The masters reading/writing from/to the memory are AXI complaint. LPDDR2 MC follows the JESD209-2F specifications. It can also be configured to power down and deep power down modes.

There are 32 read/write AXI masters, the 33rd master is the host AXI master.

The host will configure all the registers, and the device initialization of the memory will take place and then the actual read/write operation will happen. The buffer space will store all the master requests like address, data and control information, the arbiter will arbitrate the different master requests and gives grant to one master. The command generation will issue different commands to the memory like activate, read, write, precharge, refresh, power down, deep power down which

is in synchronization with the refresh and timing control block.

In this paper the LPDDR2 MC Supports SDRAM S2 and S4 devices which can be configured to 4 or 8 banks, and the capacity is 64Mb to 8 GB. The operating frequency of the memory is between 100 MHz to 533MHz.

This paper descries about the "Refresh And Timing Controller Unit" which is part of Memory controller and performs three important operations:

- Device initialization of memory device
- Refresh Control of memory device
- Timing Control for various memory related command.

2. TOP MODULE OF REFRESH AND TIMING CONTROLLER UNIT

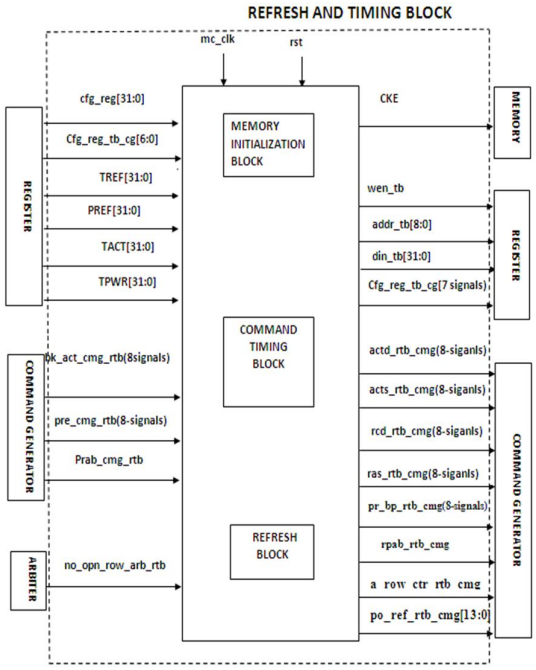

Figure 2: Top module of "Refresh And Timing Controller" unit for LPDDR2 memory controller

See Figure 2 the top module of the **"Refresh And Timing Controller" unit for LPDDR2 memory controller** , the left side signals which are input to "Refresh And Timing "block from the Registers, Arbiter and Command Generator. The right side signals which are output from "Refresh And Timing " block to the Memory, Registers and Command Generator.

There are 5 input from registers are: cfg_reg[31:0], cfg_reg_tb_cg[7:0],TACT[31:0],TPWR[31:0],TREF[31:0],PREF [31:0] ,3 inputs from command generator: bk_act_cmg_rtb(8signals),pre_cmg_rtb(8signsls),prab_cmg_rtb (1signal) , 1 input from arbiter: no_opn_row_arb_rtb and1 CKE output to memory,4 output to register wen_tb, addr_tb[8:0],din_tb[31:0],cfg_reg_tb_cg_in[7:0],

8 different output to command generator acts_bk_rtb_cmg(8signal),actd_bk_rtb_cmg(8signal),rcd_rtb_cmg(8signal),ras_rtb_cmg(8signal),pre_bp_rtb_cmg(8signal),rpab_rtb_cmg,po_ref_rtb_cmg[12:0].

3. IMPLEMENTATION OF REFRESH AND TIMING CONTROLLER UNIT

3.1 Device initialization of memory device FSM

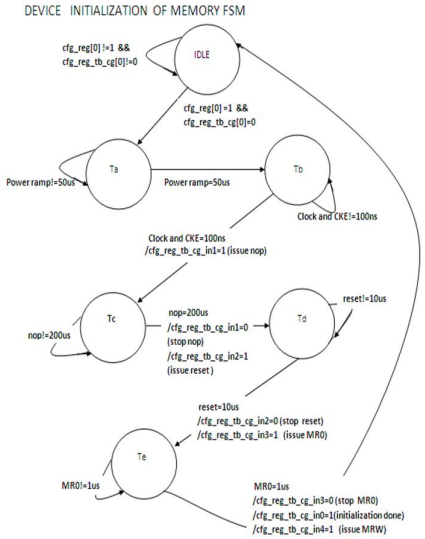

Figure 3: Device initialization of memory device FSM

See Figure 3 initialization of memory device FSM. First step in device initialization is power ramp duration minimum 50us (Ta state).Beginning (Tb State), CKE remain low for at least 100 ns. After which it is asserted high. Clock is stable at least 5 x tCK prior to the first low to high transition of CKE. While keeping CKE high, NOP commands (Tc state) is issued for at least 200 us. .After 200us is satisfied, a MRW (Reset Td-state) command is issued at least 1us is waited, while keeping CKE asserted. After 1us is satisfied(Te state) the MRR command is issued to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller will wait for a minimum of 10us before proceeding. MRW commands is used to properly configure the memory. The LPDDR2 device will now be in IDLE state and ready for any valid command.

3.2 Refresh Control of memory device FSM

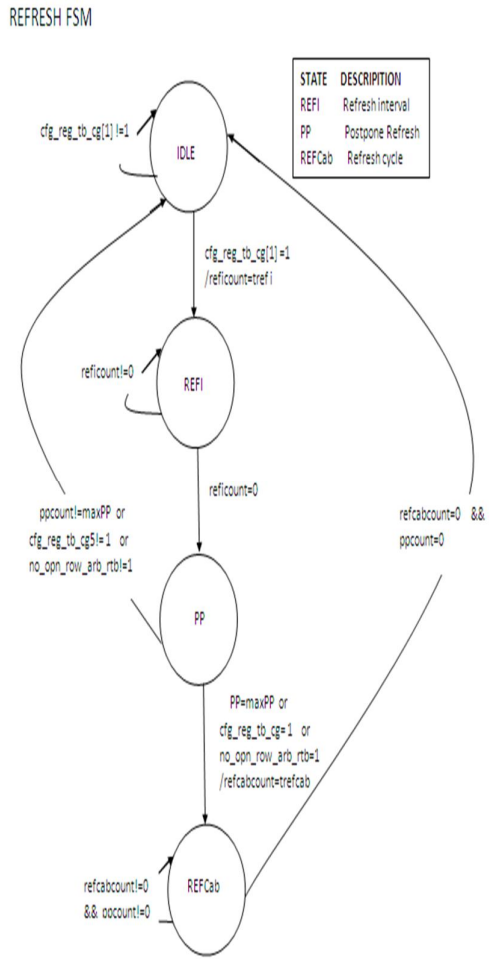

Figure4: Refresh Control of memory device FSM

See Figure 4 the refresh control of memory device FSM. Once device initialization is over it goes from idle state to refresh interval state(REFI state) in which refresh interval duration is maintied,postpone refresh is incremented each time when refresh interval is expired(PP state).When maximum postpone is reached conditional refresh is issued and refresh cycle duration is maintied(REFcab state)for number of postponed refresh.when there is no open row(no request from master to read/write) a conditional refrseh is issued.Refresh ineterval,maximum postpone duration and Refresh Cycle duuration is shown in below table 1for different memory densities.

Table 1: LPDDR2-SX : Refresh Requirements By different Device Density

Parameter	Symbol	64Mb	128Mb	256Mb	512Mb	1Gb	2Gb	4Gb	6Gb	8Gb	unit
Refresh Time in ns(tREFCab) for all Banks-	tREFCab	90	90	90	90	130	130	130	210	210	ns
Average time between REFRESH command	tREFI	15.6	15.6	15.6	15.6	7.8	7.8	7.8	3.6	3.6	us
Refresh postpone	tpp (max)	31.26	31.26	31.63	31.63	30	27.7	27.7	25.1	25.1	ms

3.3 Timing Control for various memory related command

Timing control various memory related command like activate, precharge ,power down, deep power down commands related timing are maintained in refresh and timing block. All timings which are maintained are listed in below table 2

Table 2:Different timing parameters reqiurements by different frequency

Sl.no	Parameter	Symbol	533	466	400	300	266	200	166	Freq in MHz
			1.875	2.15	2.5	3	3.75	5	6	Time period
1	ACTIVE to ACTIVE command period	tRC	tRC=tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)							
2	Row Active Time	tRAS	42							ns
3	RAS to CAS Delay	tRCD	18							ns
4	ACTIVE bank A to ACTIVE bank B	tRRD	10							ns
5	Row Active Time	tRAS	42							ns
6	Row Precharge Time(per bank)	tRPab	21							ns
7	Row Precharge Time(single bank)	tRPpb	18							ns
8	Exit power down to next valid command delay	tXP	7.5							ns
9	Minimum Deep Power Down Time	tDPD	500							us

4. SIMULATION RESULTS

4.1 Simulation of Device initialization of memory device as per figure1

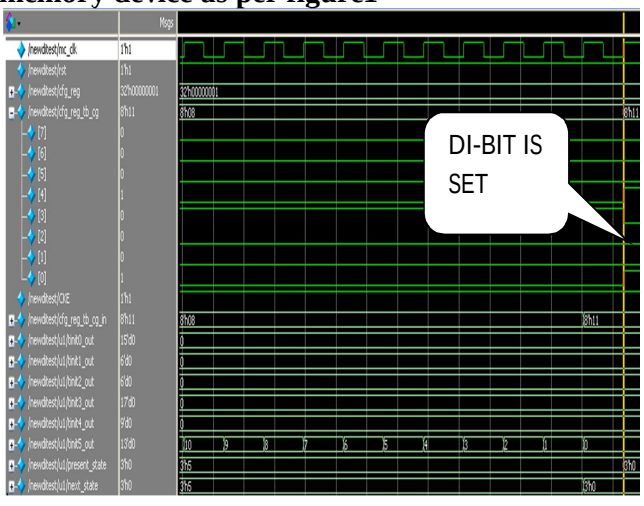

Figure 5: shows device initialization is completed by setting cfg_reg_tb_cg[0]=1(DI BIT IS SET)

4.2 Simulation of Refresh

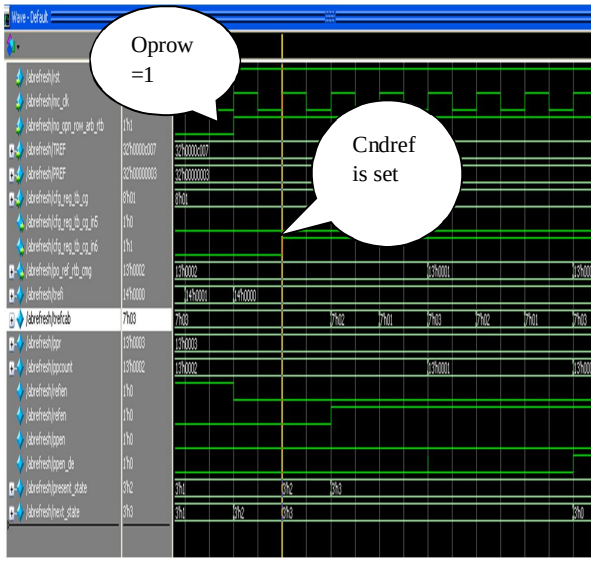

Figure 6: shows conditional refresh is issued in open row condition as per figure 3

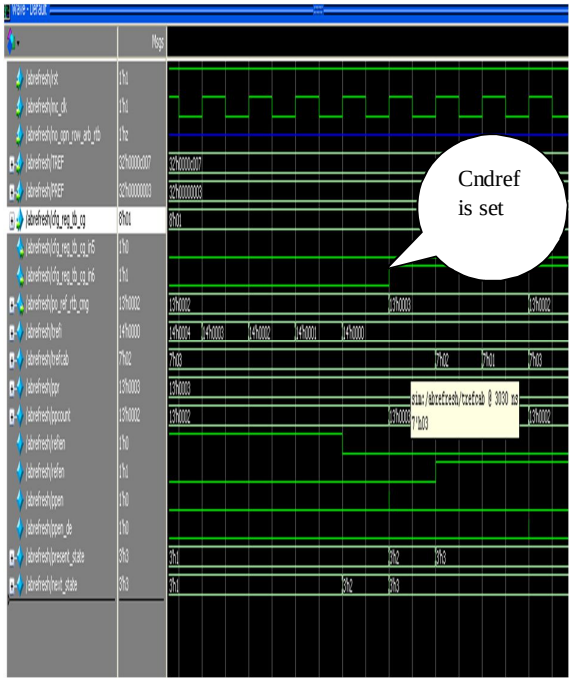

Figure 7: shows conditional refresh (Cndref is set) is issued when maximum pospone is reached as per figure 3

4.3 Simulation of Timing Control for activate command

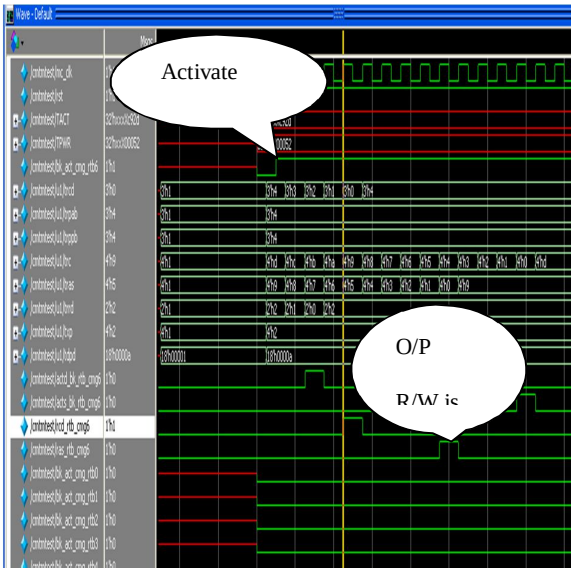

Figure 8: shows when activate command is issued and after some duration read/write bit is set and now memory can go read/write

5. CONCULSION

Device initialization of device are simulated as per JDEC spec. All timing parameters for refresh all bank, activate, precharge, power-down and deep power down command are simulated as per JDEC spec..

6. ACKNOWLEDGEMENT

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