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Methodology of Implementing the Pulse code techniques for Distributed Optical Fiber Sensors by using FPGA: Cyclic Simplex Coding

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ABSTRACT: In recent researches Coding techniques are used in OTDR approach improve Signal-to-Noise Ratio (SNR). For example, the use of simplex coding (S-coding) in conjunction with OTDR can be effectively used to enhance the Signal-to-Noise Ratio (SNR) of the backscattered detected light without sacrificing the spatial resolution; In particular, simplex codes have been demonstrated to be the most efficient among other suitable coding techniques, allowing for a good improvement in SNR even at short code lengths. Coding techniques based on Simplex or Golay codes exploit a set of different sequences (i.e. codes) of short (about 10 ns) NRZ laser pulses to increase the launched energy without impairing the spatial resolution using longer pulse width. However, the required high repetition rate of the laser pulses, hundreds of MHz for meter-scale spatial resolution, is not achievable by high peak power lasers, such as rare-earth doped fibre or passive Q-switched ones, which feature a maximum repetition rate of few hundred kHz. New coding technique, cyclic simplex coding (a subclass of simplex coding), tailored to high-power pulsed lasers has been proposed. The basic idea is to periodically sense the probing fibre with a multi-pulse pattern, the repetition period of which is equal to the fibre round-trip time. This way, the pattern results as a code spread along the whole fibre, with a bit time inversely proportional to the code length. The pulse width can be kept in the order of 10 ns to guarantee a meter-scale spatial resolution and the peak power can be set close to the nonlinear effect threshold.

Keywords: Signal, Noise, Ratio, Laser and Pulse.

I. INTRODUCTION

The purpose of this research work is to present the design and analysis of new FPGA architectures, aiming to address the main design issues related to Decoding of the averaged Stoke and Anti-Stoke traces. The main task performed by the new architecture implemented on the FPGA is to decode Stokes and anti-Stokes trace samples coming from the ADC[1][2]. The whole FPGA architecture has been developed using the Verilog hardware description language. This new FPGA architectures has three different sub-modules. Each module varies with respect to each other in terms of their functionality. The goal of the analysis is to develop FPGA architecture that can be able to decode averaged Stock and Anti-Stoke traces using minimum resource utilization. The following list is an overview of the Top-module and its three sub-module architecture considered.

A. Top Module:

The total operation of the system is performed in a single clock cycle. It is referred to as Top Module because it is the outer interface interacting with FPGA board. It takes averaged coded Stoke and Anti-Stoke trace data and codeword bit pattern, and then it returns the decoded Stoke and Anti-Stoke sampled trace data.

B. Read-Codeword Module:

All reading operations are performed in a single clock cycle. It is referred to as Read-Codeword Module because we have code word bits stored in the register. It takes code patterns and returns the code words bit by bit.

C. Read-RAM Module:

All reading operations are performed in a single clock cycle. It is referred to as Read RAM Module because there is averaged coded Stoke and Anti-Stoke sampled traces stored in the Dual port RAM. It reads the averaged Stoke and Anti-Stoke sampled traces from the Dual port RAM and returns one averaged sample per clock cycle.

D. Decoder Module

All Decoding operations are performed in a single clock cycle. It is referred to as Decoder Module because it decodes averaged coded Stoke and Anti-Stoke sampled traces. It takes both single bit codeword and single averaged Coded Stoke and Anti-Stoke sampled trace data and returns the Decoded Stoke and Anti Stoke trace data.

The contributions made by this research work include a synthesizable Verilog description of each of the module architectures described above, a synthesizable top module Verilog interface between the FPGA and the development platform used for this research.

The energy of the probing laser pulse cannot be freely increased. The energy of the launched pulse is indeed bounded by the targeted spatial resolution, which implies a small pulse width, and by the threshold for the onset of the fibre nonlinearities, which upper bounds the pulse peak power level. [11]

II. RELATED WORK

Pulse coding is the typical solution adopted to address the issues of averaging. Its basic principle is, launching proper laser pulse sequences instead of a single pulse, so as to increase the probing energy without impairing the spatial resolution.
These sequences are the optical representation of binary linear algebraic codes, which are widely used in communication theory for error detection and correction. [3]

Different codes families are grouped in to classes, each of them containing codes of the same length. Once a code class of length M is selected, a code set of M codes is built. Then, each code of the set is launched, and its Stokes and anti-Stokes responses are acquired. Finally, the set of responses is decoded to obtain a couple of Stokes and Anti-Stokes traces to be used for the temperature assessment. As described in the above, the most important aspect of pulse coding is that the SNR of decoded traces increases with M.

In particular, it had been shown that for such applications Simplex codes provide the best performance in terms of coding gain, i.e. for a given M they allow to achieve the best SNR enhancement with respect to other coding schemes [3]. It is possible to build a simplex code set for any M = 4n + 1, with n = 1, 2,3,4,....In Figure 1.1 a qualitative example for M = 3 is reported[3][4][5].

The code set is [011], [101], [110]. Whenever a laser pulse is launched, i.e. whenever the code bit is 1, a new backscattered trace starts. This means that the response R (t) to the code c acquired by the receiver is given by the overlapping of some delayed replicas of the trace (t) to be recovered [7][8][9]. The delay is a multiple of the chosen code bit time. In the reported example, the code responses are given by [10][11],

$$R_{011}(t) = \psi(t-\tau) + \psi(t-2\tau)$$
$$R_{101}(t) = \psi(t) + \psi(t-2\tau)$$
$$R_{101}(t) = \psi(t) + \psi(t-\tau)$$

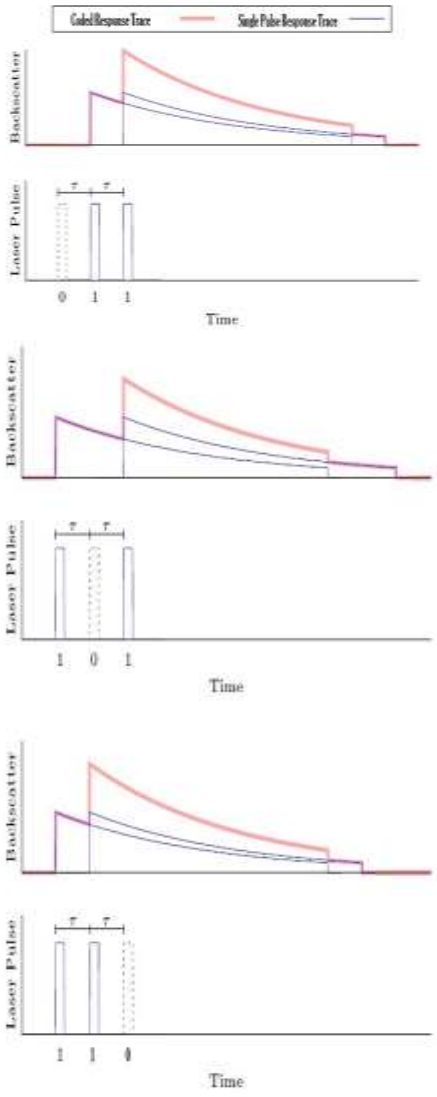

Figure 1.1. Example for Conventional Simplex Coding M = 3

Rearranging the above equations in matrix form, it follows,

$$\begin{bmatrix} R_{011}(t) \\ R_{101}(t) \\ R_{111}(t) \end{bmatrix} = S \begin{bmatrix} \psi(t) \\ \psi(t-\tau) \\ \psi(t-2\tau) \end{bmatrix} with S = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \quad \text{.... [1]}$$

III. IMPLEMENTATION

In order to evaluate the performance of FPGA based implementation, the algorithm was coded in Verilog hardware description language and implemented on Virtex4 (family using Xilinx ISE 10.0.3 tool). To test the new developed FPGA architecture and to see the real SNR improvement provided by the cyclic coding, measurements with coding are compared to the ones obtained by the conventional technique using the same acquisition time and the same peak

power, the whole DTS system has been configured. The simulation have been performed by allocating 71 bits of code words along 26 km of SMF and the repetition rate of the laser has been set to constant value. Then, extraction of the averaged Coded Stokes and Anti-Stokes trace data after 100k acquisitions (100 time-averaged traces) has been done using Lab VIEW software. Figure 1.2 shows experimental setup to acquire the coded Stokes and Anti-Stokes traces.

Figure 1.2. Experimental Setup to Acquire Coded Stokes and Anti-Stokes Traces

As described in the chapter two, Multi pulse pattern can be obtained by triggering the laser at the fixed rate and by implementing the cyclic code through an external modulator (acousto-optic Modulator), which allows to filter out a pulse if the corresponding bit code is equal to 0. This way, the pulsed laser operates at a constant frequency, which guarantees a good repeatability of the generated pulse shape and peak power.

Figure 1.3 and 1.4 shows diagram of acquired coded Stokes and anti-Stokes trace. Most of the trace recovery blocks have been implemented using Lab VIEW and others software's the likes of Microsoft-Excel

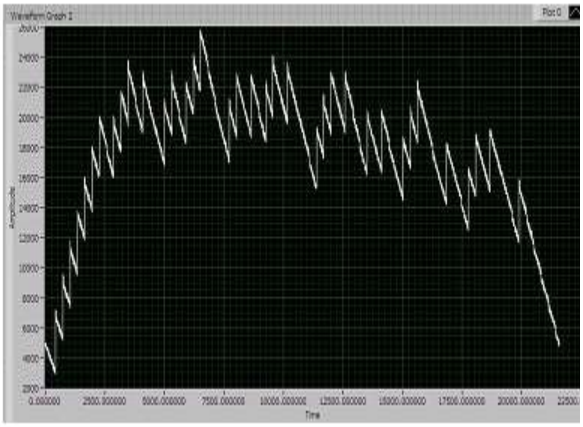

Figure 1.3. Acquired Waveform of Averaged Coded Stokes Trace, with 71 bit cyclic Simplex codes

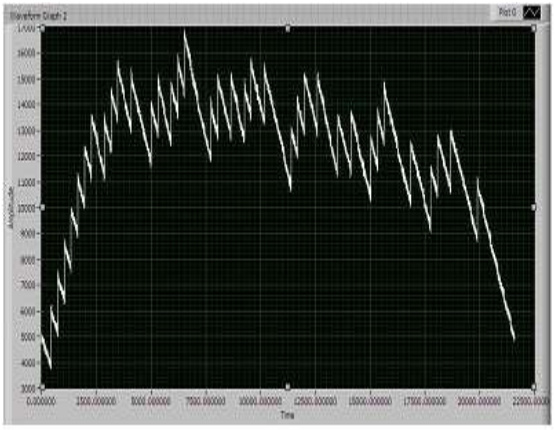

Figure 1.4. Acquired Waveform of Averaged Coded Anti-Stokes Trace, with 71 bit cyclic Simplex codes

The new FPGA architecture modules have been developed using the Verilog hardware description language. Each step of the design flow, i.e. the logical synthesis thesis, the functional simulations, the implementation and the final post place and route simulations; have been carried out within the Xilinx Integrated Software Environment (ISE) 10.1.03. Test Bench architecture that has been implemented to test multi-pulse patterns in newly developed FPGA architecture modules were carried out using Xilinx integrated Software Environment (ISE) 10.1.03. The simulation has been done with code word pattern length of 71 bit, Number of Samples per slot(number of samples for each single pulse trace in a multi-pulse technique) is 304, total number of samples (multiple of code word pattern length and Number of Samples per slot) 21584 and with working clk-frequency of 150 MHz (6 ns). Figure 1.5, 1.6 and 1.7 shows the simulation waveforms of each modules of new developed FPGA architecture.

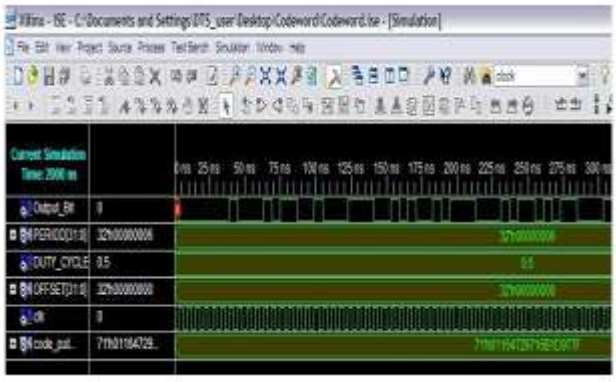

Figure 1.5 Simulation Waveform of Read-Codeword Module

Figure 1.6 Simulation Waveform of Read-RAM Module

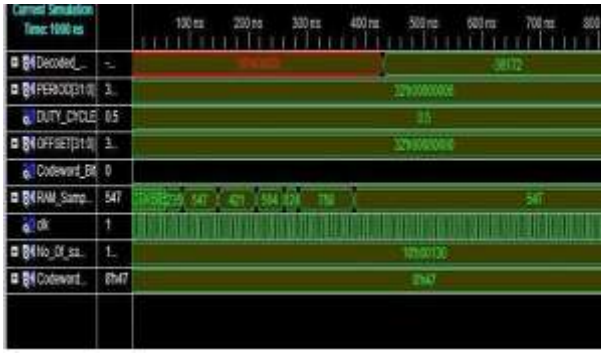

Figure 1.7 Simulation Waveform of Decoder Module

Figure 1.5, shows Simulation Waveform of Read-Codeword Module, which com- prises input of codeword bit patterns (e.g. 71 codeword bit pattern) and single bit output called output-bit.

In Figure 1.6, Simulation Waveform of Read-RAM Module is shown. It has 3 input called Number codeword bit pattern which is defined in the design phase of this thesis report, Number of Sample per Slot, (e.g 304) and clock frequency (clk). It has one output called Sample Data-out which will serve as an input for Decoder Module.

Figure 1.7, shows Simulation Waveform of Decoder Module which is the core of the new developed FPGA architecture. It takes an input from the output of the other two modules, Read-Codeword Module and Read-RAM Module. Finally it returns an output called Decoded Data, final decoded data of Averaged coded stoke and anti-stoke trace data. As a common all the three modules have an input called clock frequency (clk) which is 150 MHz (6 ns).

In figure 1.8, the utilization statistics of the Top Module (i.e. main FPGA logic resources) are shown. It can be noted that the IO Blocks are the most used which is 18%, whereas only the 2% of the available slices are occupied. This means that there is still a great room for the future development of other functionalities.

Top_Module Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	152	5472	2%
Number of Slice Flip Flops	144	10944	1%
Number of 4 input LUTs	305	10944	2%
Number of bonded IOBs	45	240	18%
Number of GCLKs	1	32	3%

Figure 1.8 FPGA Device Utilization Summary

IV. CONCLUSION

The main issues related to the design of new FPGA architecture to decode the averaged coded Stokes and Anti-Stokes multi-pulse traces data have been analyzed and addressed. This research is a small part of a large project which is undergoing at the TECIP labs of School Superior Sant'Anna. The primary focus has been on the design and implementation of decoding algorithmic module on FPGA. After describing the basic working principles of Distributed Temperature Sensor (DTS) systems, an overview of FPGA(Field Programmable Gate Array) and Verilog High level Description language has been provided, and also a new FPGA architecture which used to decode averaged coded Stokes and Anti-Stokes traces has been designed and examined in detail. Finally, the trade o s between their performance parameters has been analyzed. The new developed FPGA architecture to decode averaged coded Stoke and Anti-Stoke traces has been experimentally demonstrated and preliminary test results showed the expected performance confirming the validity of the result of embedded FPGA decoding. It lets to DTS systems an embedded decoding with less PC resources and less Overhead time for the communication to the PC. In general, laser pulse coding technique allows to significantly improving the SNR of the acquired traces. This advanced coding technique based on cyclic coding is well suited for long range DTS systems, as it can easily be implemented also with high power pulsed lasers featuring limited repetition rates.

V. REFERENCES

[1]. A. H. Hartog, "Progress in distributed fiber optic temperature sensing," in Proc. of Fiber Optic Sensor Technology and Applications Conference 2001, M. A. Marcus and B. Culshaw, Eds., vol. 4578. SPIE, 2002, pp. 4352.

[2]. D. A. Krohn, "Fiber Optical Sensors, Fundamentals and Applications, 3rd Ed" Research Triangle Park, NC, Instrument Society of America, 2000.

[3]. F. Di Pasquale "SNR enhancement of Raman based long-range distributed temperature sensors using cyclic Simplex codes" F. Baronti, A. Lazzeri, R.Roncella, R. Saletti A. Signorini, M. A. Soto, G. Bolognini,

[4]. http: ==en:wikipedia:org=wiki=Distributed Temperature Sensing.

[5]. J. M. Lopez-Higuera Ed., Handbook of Optical Fiber Sensing Technology, Chichester,U.K., John Wiley and Sons Ltd., 2001.

[6]. A. Rogers, Distributed optical fiber sensing, in Handbook of Optical Fiber Sensing Technology", J. M. Lopez-Higuera Ed. Chichester, U.K., John Wiley and Sons Ltd., 2001, ch. 14, p.271-312.

[7]. J. P. Dakin, Distributed optical fiber systems, in Optical Fiber Sensors: systems and Applications", B. Culshaw, J. Dakin, Eds. Norwood, MA, Artech House, 1988, vol.2, ch. 15, p. 575-598.

[8]. S. Adachi, "Distributed optical fiber sensors and their applications," in Proc.SICE Annual Conference, 2008, pp. 329333.

[9]. A. H. Hartog, A distributed temperature sensor based on liquid-core optical fibers, J. Lightwave Technol. 1(3), pp. 498 - 509, 1983.

[10]. S. V. Shatalin, V. N. Treschikov, A. J. Rogers, Interferometric Optical Time- Domain Reectometry for Distributed Optical-Fiber Sensing, Applied Optics.

[11]. "Raman-based distributed temperature sensor with 1m spatial resolution over 26km SMF using low-

repetition-rate cyclic pulse coding " Marcelo A. Soto,1 Tiziano Nannipieri,1 Alessandro Signorini,1 Andrea Lazzeri,2 Federico Baronti,2 Roberto Roncella,2 Gabriele Bolognini,1,* and Fabrizio Di Pasquale1.