Computer Interface for Electroluminescence (EL)

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Abstract: The goal of Computer aided device start from the physical description of integrated circuit devices, considering both the physical configuration and related device properties and build the link between the broad range of physics and electrical behavior models that support circuit design. Physics-based modeling of devices, is distributed and lumped form is an essential part of the IC process development. It seeks to quantify the underlying understanding of the technology and abstract that knowledge to the device design level, including extraction of the key parameters that support circuit design and statistical metrology [1][2]. IC development for more than a quarter-century has been dominated by the MOS technology. In the 1970s and 1980s <u>NMOS</u> was favored owing to speed and area advantages, coupled with technology limitations and concerns related to isolation, parasitic effects and process complexity. During that era of NMOS-dominated LSI and the emergence of VLSI, the fundamental scaling laws of MOS technology were codified and broadly applied [3]. It was also during this period that Computer Aided Device reached maturity in terms of realizing robust process modeling (primarily one-dimensional) which then became an integral technology design tool, used universally across the industry [4]. At the same time device simulation, dominantly two-dimensional owing to the nature of MOS devices, became the work-horse of technologists in the design and scaling of devices [5]. The transition from <u>NMOS</u> to <u>CMOS</u> technology resulted in the necessity of tightly coupled and fully 2D simulators for process and device simulations [6][7].

Keywords: Computer interface, interfacing, computer aided device.

1. INTRODUCTION

In computer science, an interface is the point of interaction with software, or computer hardware, or with peripheral devices such as a computer monitor or a keyboard. Some computer interfaces such as a touch screen can send and receive data, while others such as a mouse or microphone can only send data [8]. A hardware interfaces exist in computing systems between many of the components such as the various buses, storage devices, other I/O devices, etc. A hardware interface is described by the mechanical, electrical and logical signals at the interface and the protocol for sequencing them (sometimes called signaling). A standard interface, such as SCSI decouples the design and introduction of computing hardware, such as I/O devices, from the design and introduction of other components of a computing system, thereby allowing users and manufacturer's greater flexibility in the implementation of computing systems. Hardware interfaces can be parallel where performance is important or serial where distance is important [9]. A computer network, also referred to as just a network consists of two or more computers and typically other devices as well (such as printers, external hard drives, modems and routers), that are linked together so that they can communicate with each other and thereby exchange commands and share data, hardware and other resources. The devices on a network are referred to as nodes. They are analogous to the knots in nets that have traditionally been used by fishermen and others. Nodes can be connected using any of various types of media, including twisted pair copper wire cable, optical fiber cable, coaxial cable and radio waves. And they can be arranged according to several basic topologies (i.e., layouts), including bus (in which all nodes are connected along a single cable), star (all nodes are connected to a central node), tree (nodes successively branch off from other nodes) and ring



Pin Description of PIC16F873A microcontroller

ſ	Pin No.	Pin Name	Description		
	1	MCLR/VPP	Master Clear (input) or programming voltage		
			programming volunge		

2. DESCRIPTION OF HARDWARE

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		(output). This pin is active		
		low		
2	DAO/ANO	Digital I/O. Analog input		
2	KAU/ANU	0.		
2	D 4 1 / A N 1	Digital I/O. Analog input		
3	KA1/AN1	1.		
		Digital I/O. Analog input		
4	RA2/AN2/VREF-	2. A/D reference voltage		
4	/CVREF	(Low) input. Comparator		
		VREF output.		
	RA3/AN3/VREF+	Digital I/O. Analog input		
5		3. A/D reference voltage		
		(High) input.		
		Digital I/O- Open –Drain		
6	RA4/TOCKI/C1OUT	when configured as		
		output.		
		Digital I/O. Analog Input		
7	RA5/AN4/SS/C2OUT	4. SPI Slave selects input.		
		Comparator 2 output.		
0	VSS	Ground reference for		
8		logic and I/O Pins.		
	OSC1/CLK1	Oscillator Crystal or		
		external clock input.		
9		Oscillator crystal input or		
		external clock source		
		input		
		Oscillator Crystal or clock		
	OSC2/CLKO	output. Oscillator crystal		
10		output. Connects to		
		crystal or resonator in		
		crystal oscillator mode.		
		Digital I/O. Timer1		
11	RCO/T1OSO/T1CKI	oscillator output. Timer1		
		external clock input.		
		Digital I/O. Timer1		
12		oscillator input. Capture2		
12	KC1/11051/CC12	input, compare2 output,		
		PWM2 output.		
		Digital I/O. Capture1		
13	RC2/CCP1	input, compare 1 output,		
		PWM 1 output.		
		Digital I/O. Synchronous		
14	RC3/SCK/SCL	serial Clock input/output		
		for SPI mode.		

		Synchronous serial Clock	
		input/output for I ² C mode.	
1.5		Digital I/O. SPI data in.	
15	KC4/SDI/SDA	I ² C data I/O.	
16	RC5/SDO	Digital I/O. SPI data out.	
		Digital I/O. USART	
17	RC6/TX/CK	asynchronous transmit.	
17		USART1 synchronous	
		clock.	
	RC7/RX/DT	Digital I/O. USART	
18		asynchronous receive.	
10		USART synchronous	
		data.	
10	VSS	Ground reference for	
19		logic and I/O Pins.	
20	VDD	Positive Supply for logic	
20		and I/O Pins.	
21	RBO/INT	Digital I/O. External	
		Interrupts	
22	RB1	Digital I/O.	
23	RB2	Digital I/O.	
	RB3/PGM	Digital I/O. Low- voltage	
24		(single-supply) ICSP	
		programming enable pin.	
25	RB4	Digital I/O.	
26	RB5	Digital I/O.	
	RB6/PGC	Digital I/O. In-circuit	
27		debugger and ICSP	
		programming clock.	
	RB7/PGD	Digital I/O. In-circuit	
28		debugger and ICSP	
		programming data.	

MICROCONTROLLER PROGRAMING

PIC16F873A microcontroller used program code as given below

.....

LIST P=PIC16F873A

INCLUDE "P16F873A.INC"

BANK0 EQU 20H

	CBLOCK BANK0	SET_PO	ORTS	
	LOWERLSB		;CALL SET_PORTA	
	HIGHER		CALL SET_PORTB	
	UNIT		CALL SET_PORTC	
	TEN		RETURN	
	HUND	SET_PO	RTA	
	R1		BANKSEL ADCON1	
	R2		MOVLW 0X06	
	REQUEST		MOVWF ADCON1	
	HEX		BANKSEL TRISA	
	THOU		MOVLW 0X3F	
	TEMP		MOVWF TRISA	
	DIGIT_SEL		BANKSEL PORTA	
	DIGIT_DISP		CLRF PORTA	
	DIGIT_OUT		RETURN	
	REPEAT	SET_PO	RTB	
	ENDC		BANKSEL TRISB	
	ORG 0X000		CLRF TRISB	
RVRESE	Т		BANKSEL PORTB	
	GOTO START		CLRF PORTB	
	ORG 0X004		RETURN	
RVINT		SET_PO	RTC	
	BTFSS PIR1, ADIF		BANKSEL TRISC	
	GOTO \$-1		CLRF TRISC	
	BCF PIR1, ADIF		BANKSEL PORTC	
	CALL ADC_INT		CLRF PORTC	
	GOTO PROGRAM		RETURN	
	RETFIE	PROGRA	AM	
			CALL SET_PORTB	
START			CALL SET_PORTC	
	CALL SET_PORTS		CALL HEX_TO_BCD	
	MOVLW 0X0F		CALL NUMBER	
	MOVWF REPEAT		CALL DISPLAY	
	GOTO PROGRAM		DECFSZ REPEAT, F	

	GOTO \$-2		CLRF TRISA
	MOVLW 0X0F		COMF TRISA, F
	MOVWF REPEAT		CLRF ADRESL
	CALL REQUEST_1		NOP
	CALL ADC_1		NOP
	GOTO PROGRAM		NOP
REQUES	ST_1		NOP
	MOVLW 0X01		BANKSEL ADCON0
	MOVWF REQUEST		MOVLW 0X05
	RETURN		MOVWF ADCON0
REQUES	ST_2		GOTO \$
	MOVLW 0X09		
	MOVWF REQUEST	ADC_IN	Т
	RETURN		CALL LOW_1
REQUES	ST_3		CALL HIGH_1
	MOVLW 0X11		RETURN
	MOVWF REQUEST	LOW_1	
	RETURN		BANKSEL ADRESL
REQUES	ST_4		MOVF ADRESL, W
	MOVLW 0X19		MOVWF LOWERLSB
	MOVWF REQUEST		RETURN
	RETURN	HIGH_1	
ADC_1			BANKSEL ADRESH
	MOVLW 0XC0		MOVF ADRESH, W
	MOVWF INTCON		MOVWF HIGHER
	MOVF REQUEST, W		MOVWF HEX
	MOVWF ADCON0		RETURN
	CLRF PORTA	OUTPUT	ſ
	CLRF ADRESH		BANKSEL TRISB
	BANKSEL PIE1		CLRF TRISB
	CLRF PIE1		BANKSEL PORTB
	BSF PIE1, ADIE		MOVF HIGHER, W
	MOVLW 0X40		MOVWF PORTB
	MOVWF ADCON1		RETURN

NUMBER				RLF HEX, F	
	SWAPF UNIT, W			RLF UNIT, F	
	ANDLW 0X0F			RLF HUND, F	
	MOVWF TEN			CALL UNIT_5	
	MOVLW 0X0F			CALL TEN_5	
	ANDWF UNIT, F			BCF STATUS, 0	;8 shift
	RETURN			RLF HEX, F	
HEX_T	O_BCD			RLF UNIT, F	
	BANKSEL STATUS			RLF HUND, F	
	BCF STATUS, 0 ;1 shift			RETURN	
	RLF HEX, F		UNIT_5		
	RLF UNIT, F			MOVF UNIT, W	
	BCF STATUS, 0	;2 shift		ANDLW 0X0F	
	RLF HEX, F			MOVWF TEMP	
	RLF UNIT, F			MOVLW 0X05	
	BCF STATUS, 0	;3 shift		SUBWF TEMP, W	
	RLF HEX, F			BANKSEL STATUS	
	RLF UNIT, F			BTFSS STATUS, 0	
	CALL UNIT_5			RETURN	
	BCF STATUS, 0	;4 shift		MOVLW 0X03	
	RLF HEX, F			ADDWF UNIT, F	
	RLF UNIT, F			RETURN	
	CALL UNIT_5		TEN_5		
	BCF STATUS, 0	;5 shift		MOVF UNIT, W	
	RLF HEX, F			ANDLW 0XF0	
	RLF UNIT, F			MOVWF TEMP	
	CALL UNIT_5			MOVLW 0X50	
	BCF STATUS, 0	;6 shift		SUBWF TEMP, W	
	RLF HEX, F			BANKSEL STATUS	
	RLF UNIT, F			BTFSS STATUS, 0	
	CALL UNIT_5			RETURN	
	CALL TEN_5			MOVLW 0X30	
				ADDWF UNIT, F	
	BCF STATUS, 0	;7 shift		RETURN	

DISPLAY

CLRF DIGIT_SEL BCF DIGIT_SEL, 7 BSF DIGIT_SEL, 4 MOVF UNIT, W MOVWF DIGIT_DISP CALL S_S_DECODER MOVWF DIGIT_OUT CALL DIGIT_SELECT CALL OUT_TO_FND CALL DELAY BCF DIGIT_SEL, 4 BSF DIGIT_SEL, 5 MOVF TEN, W MOVWF DIGIT_DISP CALL S_S_DECODER MOVWF DIGIT_OUT CALL DIGIT_SELECT CALL OUT_TO_FND CALL DELAY BCF DIGIT_SEL, 5 BSF DIGIT_SEL, 6 MOVF HUND, W MOVWF DIGIT_DISP CALL S_S_DECODER MOVWF DIGIT_OUT CALL DIGIT_SELECT CALL OUT_TO_FND CALL DELAY BCF DIGIT_SEL, 6 BSF DIGIT_SEL, 7 MOVF THOU, W MOVWF DIGIT_DISP

CALL S_S_DECODER MOVWF DIGIT_OUT CALL DIGIT_SELECT CALL OUT_TO_FND CALL DELAY GOTO DISPLAY RETURN S_S_DECODER ;Display code table..... MOVF DIGIT_DISP, W ; Get key count ADDWF PCL ; and calculate jump ;NOP ; into table RETLW B'11011110' ; Code for '0' RETLW B'01000010' ; Code for '1' RETLW B'11101100'; Code for '2' RETLW B'11100110'; Code for '3' RETLW B'01110010'; Code for '4' RETLW B'10110110'; Code for '5' RETLW B'10111110'; Code for '6' RETLW B'11000010'; Code for '7' RETLW B'11111110'; Code for '8' RETLW B'11110110' ; Code for '9' ;Output display code..... RETURN OUT_TO_FND MOVF DIGIT_OUT, W MOVWF PORTB RETURN DIGIT_SELECT CLRF PORTB MOVF DIGIT SEL, W MOVWF PORTC RETURN DELAY

MOVLW 0X0F

MOVWF R1 MOVWF R2

DECFSZ R2, F

GOTO \$-1

DECFSZ R1, F

GOTO \$-4

RETURN

DELAY_L

MOVLW 0XFF

MOVWF R1

MOVWF R2

DECFSZ R2,F

GOTO \$-1

DECFSZ R1,F

GOTO \$-4

RETURN

END

3. MEASUREMENT OF ELECTROLUMINESCENCE (EL)

For the measurement of EL brightness EL cell is prepared by selected method and it is ready to use for measurement of luminescence. In prepared cell, there are two electrodes, one from conducting glass plate and other from phosphor sample side. Frequency is applied to amplifier at the desired level and it increases voltage up to required level, when frequency and voltage are reached at certain level, then emission of EL is takes place the emission of light is connected to Photomultiplier tube (PMT) and it converts the light in the form of current and then converted to voltage by voltage to current converter. The output voltage is apply to PIC16F873A microcontroller and it convert this analog voltage to Digital voltage. The digital voltage to be interfaced with the computer by parallel port. The data of parallel port is read by VB.NET software and finally luminescence of EL cell is converted in voltage, and is obtained at the screen of the computer.



Figure 1 Sample of Interfacing Window

4. REFERENCES

- H.J. DeMan and R. Mertens, SITCAP--A simulator of bipolar transistors for computer-aided circuit analysis programs, International Solid-State Circuits Conference (ISSCC), Technical Digest, pp. 104-5, February, 1973
- [2] R.W. Dutton and D.A. Antoniadis, Process simulation for device design and control, International Solid-State Circuits Conference (ISSCC), Technical Digest, pp. 244-245, February, 1979
- [3] R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rodeout, E. Bassous and A.R. LeBlanc, Design of ion-implanted MOSFETs with very small physical dimensions, IEEE Jour. Solid-State Circuits, vol. SC-9, pp.256-268, October, 1974.
- [4] R.W. Dutton and S.E. Hansen, Process modeling of integrated circuit device technology, Proceeding IEEE, vol. 69, no. 10, pp. 1305-1320, October, 1981.
- [5] P.E. Cottrell and E.M. Buturla, "Two-dimensional static and transient simulation of mobile carrier transport in a semiconductor," Proceedings NASECODE I (Numerical Analysis of Semiconductor Devices), pp. 31-64, Boole Press, 1979.
- [6] C.S. Rafferty, M.R. Pinto, and R.W. Dutton, Iterative methods in semiconductor device simulation, IEEE Trans. Elec. Dev., vol. ED-32, no.10, pp.2018-2027, October, 1985.
- [7] M.R. Pinto and R.W. Dutton, Accurate trigger condition analysis for CMOS latchup, IEEE Electron Device Letters, vol. EDL-6, no. 2, February, 1985.
- [8] IEEE 100 The Authoritative Dictionary Of IEEE Standards Terms. NYC, NY, USA: IEEE Press. 2000. pp. 574–575. ISBN 0-7381-2601-2.
- Blaauw, Gerritt A.; Brooks, Jr., Frederick P. (1997), "Chapter 8.6, Device Interfaces", Computer Architecture-Concepts and Evolution, Addison-Wesley, pp. 489–493, ISBN 0-201-10557-8 See also:

Patterson, David A.; Hennessey, John L. (2005), "Chapter 8.5, Interfacing I/O Devices to the Processor, Memory and Operating System",

Computer Organization and Design - The Hardware/Software Interface, Third Edition, Morgan Kaufmann, pp. 588–596, ISBN 1-55860-604-1