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Design of High Speed Phase Frequency Detector in 0.18 µm CMOS Process for PLL Application

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Abstract:

The Phase Frequency Detectors (PFD's) are proposed in this research paper by using the two different structures of D Flip-Flop that is the traditional D Flip-Flop and modified D Flip-Flop with a NAND gate which can overcome the speed and area limitations of the conventional PFD. Both of the PFD's use 20 transistors. The traditional PFD consumes 133.92 µW power when operating at 40 MHz frequency with 1.8 Volts supply voltage whereas the modified PFD consumes 100.51 µW power operating at 40 MHz frequency with 1.8 Volts supply voltage. The designs are implemented by using 0.18 meter CMOS process in Tanner 13.ov. These can be used in PLL for high speed applications.

Keywords: CMOS, Phase Locked Loop (PLL), D Flip-Flop, Phase Frequency Detector (PFD), NAND gate, Clock Signal

1. INTRODUCTION:

PFD is one of the main blocks of the PL which is used in various applications such as Wireless Communication systems. Digital Circuits, Sensor Receivers etc. The implementation of a fully integrated, low power and high performance PLL significantly affect the overall system performance [1][2].

In the PLL, the Phase Frequency Detectors (PFD's) compares the rising edges of the reference clock and the voltage controlled oscillator (VCO) clock, and generates a lead signal when the reference phase is leading or a lag signal when the reference phase is lagging [2][3]. The phase difference which is detected in the PFD passes through the loop filter to control the VCO.As the phase difference critically affects the overall characteristics of the PLL such as the lock in time and jitter performance, the PFD should be designed in order to work accurately for any phase difference [1][2][4].

The design of PFD consists of two flip-flops and NAND gate to provide a reset path [3][4]. As shown in Figure 1, the D input of the flip-flops is connected to high and the input signals are applied to the clock input. When one of the clock changes to high, this flip-flop will be charged and change its output to high [4][5]. The NAND gate is for preventing both the flip-flops to be high at the same time. As we can see the inputs of the NAND gate are both Up and Down signal from both the flip-flops and the output of the NAND gate is connected to the

reset input of the flip-flops. As soon as both the outputs (Up and Down) are high the NAND gate will generate a high signal that will reset both flip-flops by avoiding the situation of both high at the same time [5][7].

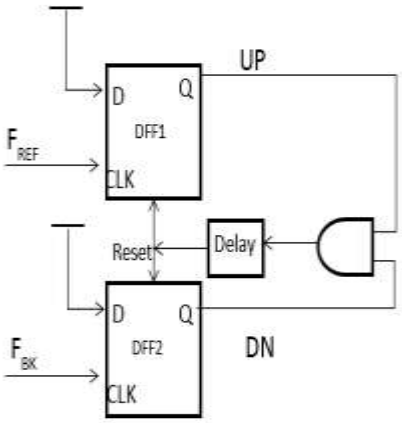

Figure 1 Block Diagram of PFD

The following figures Figure 2 and Figure 3 shows the schematic diagram of traditional and the modified D Flip-Flop respectively which is used to design the architecture of traditional and modified PFD [6][7].

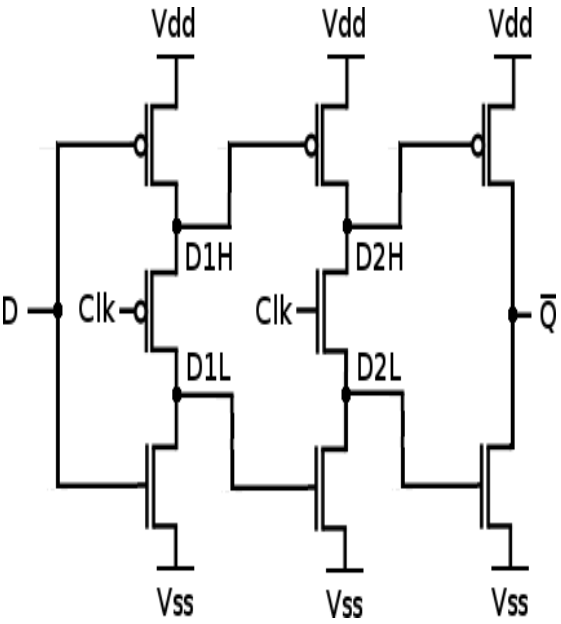

Figure 2 Schematic Diagram of Traditional D Flip-Flop

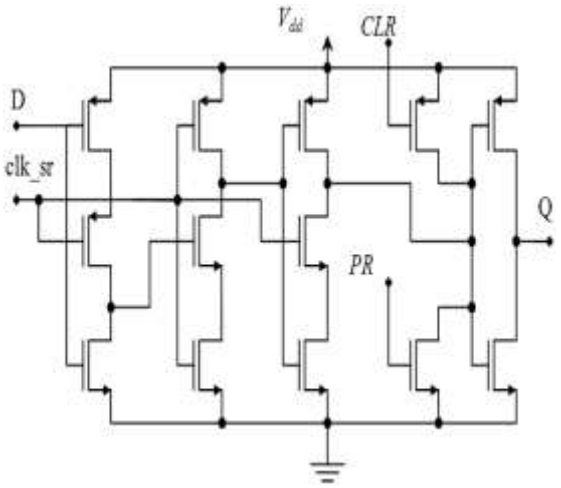

Figure 3 Schematic Diagram of Modified D Flip-Flop

2. TRADITIONAL PHASE FREQUENCY DETECTOR:

This research paper presents two PFD architectures having low area and can work on higher frequencies [7][8]. Figure 4 shows the Phase Frequency Detectors (PFD's by using NAND gate). The circuit consists of two resettable, edge triggered traditional D Flip-Flops with their D inputs tied to logic 1 [6][7]. The CLK1 and CLK serve as the clocks of the flip-flops. Suppose the rising edge of CLK1 leads that of CLK, then UPb goes to logic high. UPb keeps high until the rising edge of the CLK makes DNb on high level. Because UPb and DNb are NANDed, so RESET goes to logic high and resets the PFD into the initial state [6][7][8]. The schematic of NAND gate based PFD circuit consisting of only 20 transistors is as given in Figure 4.

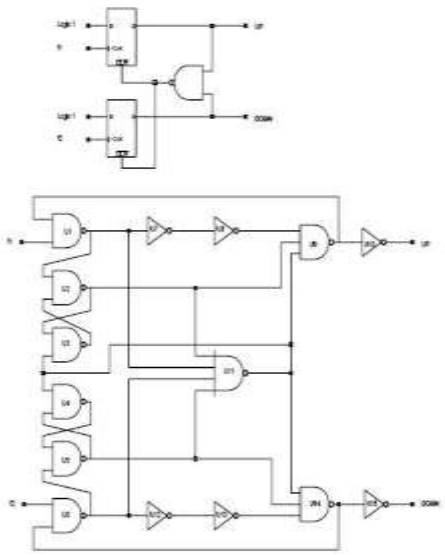

Figure 4 Schematic Diagram of Traditional PFD by using NAND Gates

3. MODIFIED PHASE FREQUENCY DETECTOR:

Figure 5 shows the phase frequency detector by using NAND gate. The circuit consists of two resettable, edges triggered D flip-flops with their D inputs tied to logic 1. The CLKREF and CLK serve as the clocks of the flip-flops. The UPb and DNb signals are given as input to the NAND gate. Suppose the rising edge of CLKREF leads that of CLK, then UPb goes to logic low i.e. Up keeps high until the rising edge of CLK makes DNb on low level [7][8]. Because UPb and DNb are NORed, so RESET goes to logic high and resets the PFD into the initial state. The circuit is implemented by using 0.18 µm CMOS process in Tanner 13.0v with only 20 transistors.

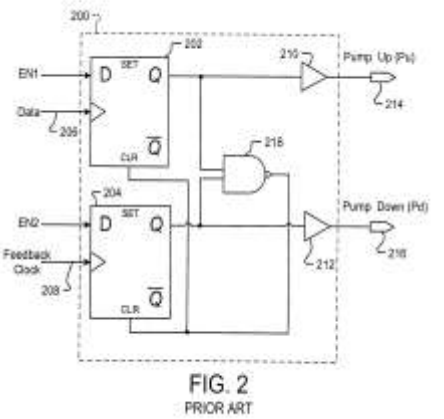

FIG. 2
PRIOR ART

Figure 5 Schematic Diagram of Modified PFD by using NAND Gates

4. SIMULATION AND RESULTS:

Both the PFD circuits are simulated on Tanner 13.0 at 1.8Volts in order to obtain the results

with the input frequency of 40 MHz [2][3][8]. The NAND gate based PFD circuit is simulated on Tanner 13.0 at 1.8 Volts in order to obtain the results with the input frequency of 40 MHz as shown in Figure 6.

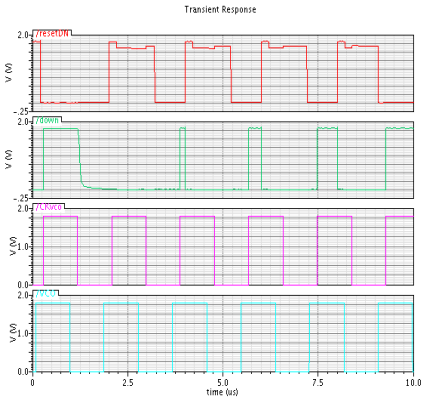

Figure 6 Waveforms of NAND Gate-Based Traditional PFD

The NAND gate based modified PFD circuit is simulated on Tanner 13.0 at 1.8 Volts in order to obtain the results with the input frequency of 40 MHz as shown in Figure 7.

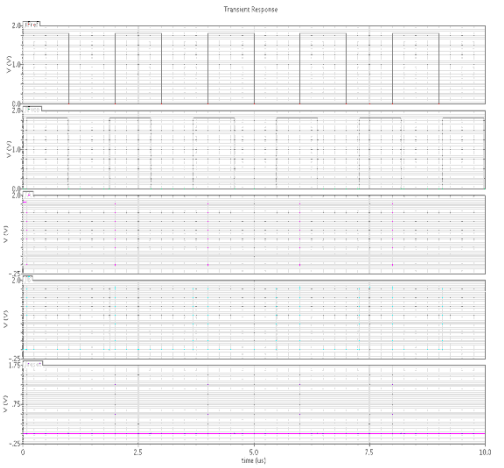

Figure 7 Waveforms of NAND Gate-Based Modified PFD

The two circuits can be simulated when the Free and Face have different frequencies [3][4][5]. Figure shows the waveform for NAND gate based PFD. The Up signal and the DN signal go high at the rising edge of Free and Face. When both Up and Dn signals become logic high the circuit is reset to the initial state. The pulse width of the UP and DN signal is proportional to the frequency difference between the two inputs [4][5][7].

5. PERFORMANCE AND COMPARISON:

Type of PFD	Operating Frequency	No. of Transistors	Power Consumption	Delay	Dead Zone
Traditional PFD	40 MHz	20	133.91 µW	10 ns	9 ps
Modified PFD	40 MHz	20	100.51 µW	10 ns	1 ps

6. CONCLUSION:

This research paper presents two PFD designs which are implemented in the 0.18 µm CMOS process. Both of the PFD consists of only 20 transistors and can operate up to 1 GHz frequency but the modified PFD preserves the main functionality of traditional PFD with low power consumption.. The dead zone of traditional PFD is 9 ps whereas for modified PFD is 6 ps. The performance of the two PFD's is compared against the traditional PFD in Table 1.

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8. REFERENCES:

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