

Intel Microprocessors- a Top down Approach

Muhammad Irfan¹, Jan Sher¹, Naveed Ullah¹, Muhammad Sulaiman¹, Junaid Saleem¹
¹Department of computer science, Abdul Wali Khan University Mardan, KPK, Pakistan

Abstract- IBM is the world's largest manufacturer of computer chips. Although it has been challenged in recent years by newcomers AMD and Cyrix, Intel still Predominate the market for PC microprocessors. Nearly all PCs are based on Intel's x86 architecture. IBM (International Business Machines) is by far the world's largest information technology company in terms of Gross (\$88 billion in 2000) and by most other measures, a position it has held for about the past 50 years. IBM products include hardware and software for a line of business servers, storage products, custom-designed microchips, and application software. Increasingly, IBM derives revenue from a range of consulting and outsourcing services. In this paper we will compare different technologies of computer system, its processor and chips.

Keywords: Intel, Microprocessor, Server, PCs

I. INTRODUCTION

Intel is the American company headquartered in Santa Clara, California. Intel is one of the world largest and highest valued semiconductor chip makers, based on Gross. It is the Discoverer of the x86 series of microprocessors, the processors found in most personal computers. Intel supplies processors for computer system manufacturers such as Apple, Samsung, HP and Dell. Intel also makes motherboard chipsets, network interface controllers and integrated [1, 2] circuits, flash memory, graphics chips, embedded processors and other devices related to communications and computing. Intel Corporation was founded on July 1968 by semiconductor Innovators Robert Noyce and Gordon Moore and to a great degree associated with the executive (Administrator) leadership and Imagination of Andrew Grove, Intel combines advanced chip design capability with a leading-edge manufacturing capability. Intel was an early developer of SRAM and DRAM memory chips [3-8], which represented the majority of its business until 1981. Although Intel created the world's first commercial microprocessor chip in 1971, it was not

until the success of the personal computer (PC) that this became its primary business. During the 1990s, Intel invested heavily in new microprocessor designs fostering the rapid growth of the computer industry During this period Intel became the dominant supplier of microprocessors for PCs, and was known for aggressive and anti-competitive tactics in defense of its market position, particularly against Advanced Micro Devices (AMD), as well as a struggle with Microsoft for control over the direction of the PC industry.

II. HARDWARE SPECIFICATIONS

We'll compare Intel's Xeon E5-2698 v3 (Haswell) and IBM's ISeries 8286-42A (POWER8) processors for our test applications. The test application is a Monte-Carlo simulation, pricing a portfolio of LIBOR swaptions [9-14] and simultaneously computing first order sensitivities (Greeks) to the initial forward rates using path-wise Adjoint Algorithmic Differentiation (AD). The LIBOR market model is applied to simulate thousands of possible future development paths for the LIBOR forward rates, using normally-distributed random numbers. Within each of these Monte-Carlo paths, the value of the swaption portfolio [15] is then calculated by applying a portfolio payoff function. For ad joint differentiation, the algorithm is then executed in reverse to find the Greeks. To obtain the final results, both the price and the Greeks are averaged across all paths [16, 17].

The processing graph in Figure 1 illustrates the application:

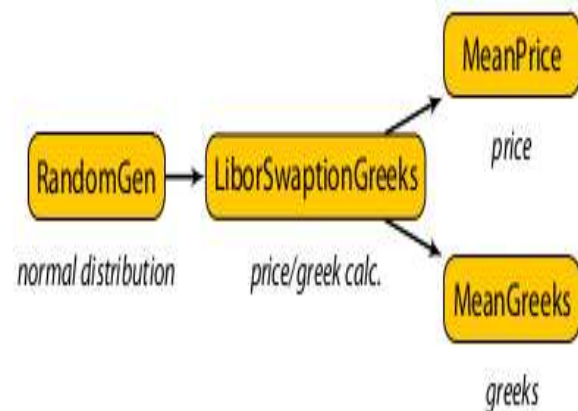


Figure 1: Processing Graph

III. BENCHMARK SETUP

The test systems had the following configuration:

- **CPU:** 2x Intel Xeon E5-2698 v3 (HT on) and 2 x POWER8 8286-42A (SMT on)
- **OS:** RedHat Enterprise Linux 6.6 and Ubuntu 14.10
- **RAM:** 256GB
- **Compiler:** Intel Compiler 15.0 and IBM Compiler 13.1

The application was compiled with maximum optimization settings, fast math mode, and tuning for the target processor architecture. The generated code makes extensive use of low-level processor features, such as vector extensions, fused [17-22] multiply-add instructions, cache optimizations, etc.

IV. INTEL vs. IBM

POWER8-based uniprocessor/dual processor systems can execute more work more quickly than Intel E5 v2 Xeon-based servers. POWER8 can process four times as many threads as its E5 v2 competitors; the POWER8 clock speed is faster; and POWER8 can work on significantly more data in cache than E5 v2-based servers. Furthermore, POWER8 memory bandwidth is much faster than the Intel environment. What all of this means is that POWER8-based servers can outperform E5 v2-based servers (helping enterprises achieve results more quickly); and POWER8-based servers are also more efficient (meaning that enterprises will not need to buy as many servers to execute workloads. This will help enterprises save BIG MONEY by not having to purchase as many software licenses).

1. Both microprocessor/server environments have been designed to process Web, file and print, email, database, vertical-specific applications, high performance computing and cloud workloads;
2. POWER8 processors are more efficient than Xeon processors;
3. Due to processing and bandwidth advantages, POWER8-based servers can deliver results more quickly.
4. POWER8-based servers are better suited for data-intensive environments; and,
5. When executing identical workloads, POWER8-based servers will cost less than E5 v2-based competitors (due to aggressive IBM pricing and numerous efficiency advantages).

V. BACKGROUND

In June, 2013, Intel released the first member of its dual processor E5 v2 family – the Xeon E5-2692 v2 (Intel now offers 38 different E5 v2 processors that operate at varying

speeds, with from four to fifteen cores per processor). These processors have been designed largely to serve the Windows and Linux marketplaces [23-28]. There is a lot to like about this family of microprocessors as compared with the previous Xeon generation because these processors (codenamed “Ivy Bridge”) offer more cores, more cache, faster speed, lower energy consumption, and reliability/availability/serviceability extensions). But probably the biggest improvement in Xeon v2 architecture is the amount of main memory that can now be addressed [29-33]. With v2 architecture, x86 servers will

Someday be able to address up to 16TB of main memory in large, scale-up configurations. Clabby Analytics is impressed with both architectures. We like the way Intel has finally addressed the memory limitations of scale-up x86 architectures (the subject of this report). But we are especially impressed with the processor efficiency, performance and bandwidth improvements offered with POWER8-based systems. With a faster clock speed; with the ability to process four times as many threads per cycle as x86 processors; with three times more on-chip cache; with four to six times the memory bandwidth – and with access to up to 80 TB of Flash using the newly introduced coherence attached processor interface (CAPI) – IBM has created a systems environment with POWER8 that has been designed to very significantly outperform Intel Xeon architecture. The way we see it, this new generation of POWER8-based servers has literally been “designed for data”. We see the current generation of single and dual-socket systems as a true threat to the x86 dominance of the scale-out Linux marketplace. And, as larger and large configurations come to market, we expect to see a lot of POWER8-based servers configured for large database-in-memory processing – and given POWER8 performance advantages, these new in-memory servers will raise the performance bar for database processing in the future. The Primary Differentiators: Performance and Efficiency As we compared Intel’s Xeon E5-2692 v2 with IBM’s POWER8 architecture from both a processor design and subsystem perspective [34], it became readily apparent that both chips were designed to process serial, parallel and data-intensive workloads – but it also became clear that IBM’s POWER8 architecture was designed to deliver high-performance while operating far more efficiently [35] than Intel’s Xeon architecture.

To illustrate these points, consider the following: Performance – IBM’s POWER8 is more than 25% faster per clock cycle than Intel’s E5-2692 v2 (IBM operates at 4.15 GHz per clock cycle; Intel’s E5-2692 v2 runs at 2.697 GHz). POWER8 offers three times more on-chip cache (data in cache can be read faster – leading to faster performance and faster results). Further, POWER8 can address almost 25% more main memory than the E5-2692 v2 – again placing more data closer to the processor where it can be read and acted-on more quickly. And POWER8 can receive data from memory four to six times faster than Xeon bus can. The combination of a faster processor with access to more cache and memory – with significantly faster memory bandwidth – make POWER8 processors more powerful than Xeon E5 architectures. Efficiency – POWER8 offers a 12 core

processor configuration that can process 8 threads per core (or 96 threads simultaneously per clock cycle). By comparison, Intel's E5-2697) has 12 cores but can only process two threads per core for a total of only 24 threads per clock cycle. This one design difference – processor efficiency – is extremely important when comparing POWER architecture to Xeon x86 architecture. A single 12 core POWER8 processor can process over three times as much data per clock cycle as compared to a 12 core Xeon E5-2697. What this means is that it could take up to three Xeon servers to do the work of a single POWER8-based server. It also means x86 buyers would potentially need to purchase up to three times the number of software licenses when opting for a Xeon-based server solution. Figure 2 presents a side-by-side comparison of Intel's Xeon E5-2697 v2 versus IBM's POWER8 architecture. Especially important to note are: 2. The # of threads/core (POWER8 can process 8 threads per core per clock cycle to Intel's two threads) – this gives IBM a huge processor efficiency advantage over Xeon;

The amount of data that can be placed in cache (POWER8 offers over three times as much cache). It should also be noted that POWER8 can also make use of 128 MB eDRAM L4 cache that resides just off the chip. All of this close-proximity cache gives IBM's POWER8 a huge data processing speed advantage over Intel's Xeon E5 architecture; and, 3. The memory bandwidth speed (POWER8 is almost four times faster than Xeon).

In addition to huge performance and efficiency advantages, IBM has also "CAPI-enabled" its POWER8 processors. With POWER8, IBM has placed PCIe Gen 3 logic directly on the chip – and has built an interface to this logic known as the coherence attached processor interface (or CAPI). As illustrated in Figure 2, CAPI is a customizable hardware accelerator that enables devices, Flash and coprocessors to talk directly and at very high speeds with POWER8 processors. Xeon offers a similar interface known as Quick Path Interconnect (QPI) – the primary differentiator [36] is that CAPI is an open interface while QPI is not.

VI. SUMMARY OBSERVATIONS

When selecting computer systems, the primary goal of information technology (IT) decision makers should be to pick the computer system best suited to most efficiently execute assigned workloads. By choosing the right information systems IT executives can lower computing costs (because fewer computing systems are needed, and because fewer software licenses will be required). Further, more efficient systems often yield faster computing results (a Quality-of-Service [QoS] consideration). Accordingly, the choice of infrastructure (microprocessors, system designs, systems software) matters tremendously. The major differentiators when comparing Xeon 35 v2 processors with POWER8 microprocessors can be found in performance and efficiency:

1. Performance – POWER8's clock speed is almost 25% faster than the E5-2692; it has access to three times more on-chip cache – and data in memory can be fed to POWER8 which is four times faster than

its Xeon competitor. This kind of optimization makes POWER8 a Formidable competitor – especially when running data-intensive applications.

2. Efficiency – When running the same workload on a POWER8 as compared with a Xeon E5 Competitor, expect more work to be processed per clock cycle (to be precise, expect three Infrastructure Matters: POWER 8-based Power Systems vs. x86 Servers
3. Times as much work to be processed per clock cycle). Because POWER8 can process more work More quickly, expect to have to use fewer POWER8-based systems to handle an identical workload (Or expressed differently, expect to need to purchase up to three Xeon E5-based servers to handle
4. The same amount of work as a POWER8-based server. Also expect to spend up-to three times more money for additional software licenses). IBM's POWER8 announcement focused quite a bit on the performance and efficiency benefits that Can be derived by adopting POWER8-based scale-out Power Systems. But we are also intrigued by some of the new innovations taking place within the Power Systems. At Clabby Analytics, we Believe that, over the next several years, hundreds of new hybrid coprocessor products will come to market – bringing new innovations and new performance deltas along with them. The comparison is shown in Table 1.

VII. PERFORMANCE COMPARISON

	Intel Xeon E5-2697v2	powers8
Processor speed	2.697 GHZ	4.15 GHZ
Cores(singale socket)	12	12
Threads/core	2	8
Max main memory	768G	1Tb
Memory controllers	1	2
Level 1	32Kbi+32kbD/core	64 kb/core
Level 2	256KB/core	512KB/core
Level 3	30MB/chip	96MB/chip
Memory bandwidth	59.7GB/s	230GB/s 486

We compared the computation times of the test application on both processors, excluding the random number generation as shown in Figure 2. The test swaption portfolio consists of 15 trades and 80 forward LIBOR rates are Table 1: Comparison between Intel and Power 8

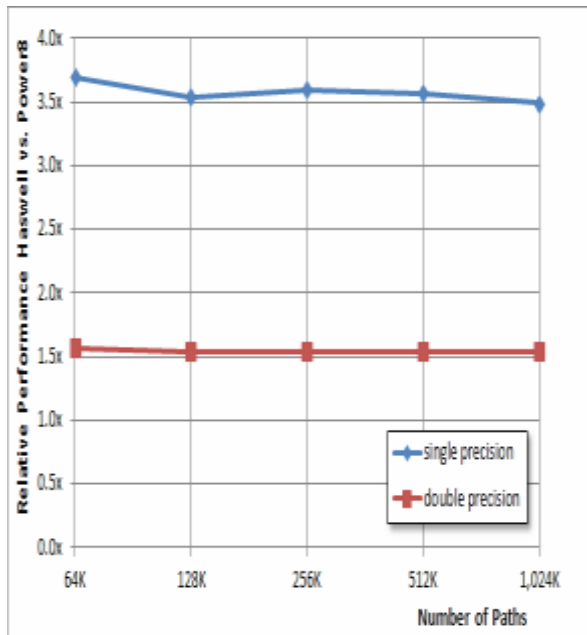


Figure 2: Comparison in terms of Performance

VIII. CONCLUSION

In this paper, we made a comparison between various Intel microprocessors. We briefly explain the history and various categories and also evaluate them based on their performance. Not so long ago, processors were judged largely by raw clock speed alone, a measure of how many calculations the chip is capable of performing in the space of a second. These days, it's all about cores, which have allowed chipmakers like Intel to boost speed by splitting tasks across a number of processing units that exist on the same die. Coupled with software designed to take advantage of multiple cores, such processors can wind up tackling intensive work faster than ever before.

REFERENCES

- [1]. Khan, F., Bashir, F., & Nakagawa, K. (2012). Dual Head Clustering Scheme in Wireless Sensor Networks. in the IEEE International Conference on Emerging Technologies (pp. 1-8). Islamabad: IEEE Islamabad.
- [2]. M. A. Jan, P. Nanda, X. He, Z. Tan and R. P. Liu, "A robust authentication scheme for observing resources in the internet of things environment" in 13th International Conference on Trust, Security and Privacy in Computing and Communications (TrustCom), pp. 205-211, 2014, IEEE.
- [3]. Khan, F., & Nakagawa, K. (2012). Performance Improvement in Cognitive Radio Sensor Networks. in the Institute of Electronics, Information and Communication Engineers (IEICE) , 8.
- [4]. M. A. Jan, P. Nanda and X. He, "Energy Evaluation Model for an Improved Centralized Clustering Hierarchical Algorithm in WSN," in *Wired/Wireless Internet Communication, Lecture Notes in Computer Science*, pp. 154–167, Springer, Berlin, Germany, 2013.
- [5]. Khan, F., Kamal, S. A., & Arif, F. (2013). Fairness Improvement in long-chain Multi-hop Wireless Adhoc Networks. International Conference on Connected Vehicles & Expo (pp. 1-8). Las Vegas: IEEE Las Vegas, USA.
- [6]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "Enhancing lifetime and quality of data in cluster-based hierarchical routing protocol for wireless sensor network", 2013 IEEE International Conference on High Performance Computing and Communications & 2013 IEEE International Conference on Embedded and Ubiquitous Computing (HPCC & EUC), pp. 1400-1407, 2013.
- [7]. Q. Jabeen, F. Khan, S. Khan and M.A Jan. (2016). Performance Improvement in Multihop Wireless Mobile Adhoc Networks. in the *Journal Applied, Environmental, and Biological Sciences (JAEBS)*, vol. 6(4S), pp. 82-92. Print ISSN: 2090-4274 Online ISSN: 2090-4215, TextRoad.
- [8]. Khan, F., & Nakagawa, K. (2013). Comparative Study of Spectrum Sensing Techniques in Cognitive Radio Networks. in *IEEE World Congress on Communication and Information Technologies* (p. 8). Tunisia: IEEE Tunisia.
- [9]. Khan, F. (2014). Secure Communication and Routing Architecture in Wireless Sensor Networks. the 3rd Global Conference on Consumer Electronics (GCCE) (p. 4). Tokyo, Japan: IEEE Tokyo.
- [10]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "PASCCC: Priority-based application-specific congestion control clustering protocol" *Computer Networks*, Vol. 74, PP-92-102, 2014.
- [11]. Khan, F. (2014, May). Fairness and throughput improvement in multihop wireless ad hoc networks. In *Electrical and Computer Engineering (CCECE), 2014 IEEE 27th Canadian Conference on* (pp. 1-6). IEEE.
- [12]. Mian Ahmad Jan and Muhammad Khan, "A Survey of Cluster-based Hierarchical Routing Protocols", in *IRACST–International Journal of Computer Networks and Wireless Communications (IJCNC)*, Vol.3, April. 2013, pp.138-143.
- [13]. Khan, S., Khan, F., & Khan, S.A.(2015). Delay and Throughput Improvement in Wireless Sensor and Actor Networks. 5th National Symposium on

- Information Technology: Towards New Smart World (NSITNSW) (pp. 1-8). Riyadh: IEEE Riyadh Chapter.
- [14]. Khan, F., Khan, S., & Khan, S. A. (2015, October). Performance improvement in wireless sensor and actor networks based on actor repositioning. In *2015 International Conference on Connected Vehicles and Expo (ICCVE)* (pp. 134-139). IEEE.
- [15]. Khan, S., Khan, F., Jabeen, Q., Arif, F., & Jan, M. A. (2016). Performance Improvement in Wireless Sensor and Actor Networks. in the Journal Applied, Environmental, and Biological Sciences Print ISSN: 2090-4274 Online ISSN: 2090-4215
- [16]. Mian Ahmad Jan and Muhammad Khan, "Denial of Service Attacks and Their Countermeasures in WSN", in *IRACST-International Journal of Computer Networks and Wireless Communications (IJCNCW)*, Vol.3, April. 2013.
- [17]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "A Sybil Attack Detection Scheme for a Centralized Clustering-based Hierarchical Network" in *Trustcom/BigDataSE/ISPA*, Vol.1, PP-318-325, 2015, IEEE.
- [18]. Jabeen, Q., Khan, F., Hayat, M.N., Khan, H., Jan., S.R., Ullah, F., (2016) A Survey : Embedded Systems Supporting By Different Operating Systems in the International Journal of Scientific Research in Science, Engineering and Technology(IJSRSET), Print ISSN : 2395-1990, Online ISSN : 2394-4099, Volume 2 Issue 2, pp.664-673.
- [19]. Syed Roohullah Jan, Syed Tauhid Ullah Shah, Zia Ullah Johar, Yasin Shah, Khan, F., " An Innovative Approach to Investigate Various Software Testing Techniques and Strategies", International Journal of Scientific Research in Science, Engineering and Technology(IJSRSET), Print ISSN : 2395-1990, Online ISSN : 2394-4099, Volume 2 Issue 2, pp.682-689, March-April 2016. URL : <http://ijsrset.com/IJSRSET1622210.php>
- [20]. Khan, F., Jan, SR, Tahir, M., & Khan, S., (2015) Applications, Limitations, and Improvements in Visible Light Communication Systems" In *2015 International Conference on Connected Vehicles and Expo (ICCVE)* (pp. 259-262). IEEE.
- [21]. Syed Roohullah Jan, Khan, F., Muhammad Tahir, Shahzad Khan,, (2016) "Survey: Dealing Non-Functional Requirements At Architecture Level", *VFAST Transactions on Software Engineering*, (Accepted 2016)
- [22]. M. A. Jan, "Energy-efficient routing and secure communication in wireless sensor networks," Ph.D. dissertation, 2016.
- [23]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Lightweight Mutual Authentication Scheme for IoT Objects," *IEEE Transactions on Dependable and Secure Computing (TDSC)*, "Submitted", 2016.
- [24]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Sybil Attack Detection Scheme for a Forest Wildfire Monitoring Application," *Elsevier Future Generation Computer Systems (FGCS)*, "Accepted", 2016.
- [25]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2015, August). DPBSV--An Efficient and Secure Scheme for Big Sensing Data Stream. In *Trustcom/BigDataSE/ISPA*, 2015 IEEE (Vol. 1, pp. 246-253). IEEE.
- [26]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2015). A Dynamic Key Length Based Approach for Real-Time Security Verification of Big Sensing Data Stream. In *Web Information Systems Engineering--WISE 2015* (pp. 93-108). Springer International Publishing.
- [27]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2016). A dynamic prime number based efficient security mechanism for big sensing data streams. *Journal of Computer and System Sciences*.
- [28]. Puthal, D., & Sahoo, B. (2012). Secure Data Collection & Critical Data Transmission in Mobile Sink WSN: Secure and Energy efficient data collection technique.
- [29]. Puthal, D., Sahoo, B., & Sahoo, B. P. S. (2012). Effective Machine to Machine Communications in Smart Grid Networks. *ARNP J. Syst. Softw.* © 2009-2011 *AJSS Journal*, 2(1), 18-22.
- [30]. M. A. Jan, P. Nanda, M. Usman, and X. He, "PAWN: A Payload-based mutual Authentication scheme for Wireless Sensor Networks," "accepted", 2016.
- [31]. M. Usman, M. A. Jan, and X. He, "Cryptography-based Secure Data Storage and Sharing Using HEVC and Public Clouds," *Elsevier Information sciences*, "accepted", 2016.
- [32]. Jan, S. R., Khan, F., & Zaman, A. THE PERCEPTION OF STUDENTS ABOUT MOBILE LEARNING AT UNIVERSITY LEVEL. *NO. CONTENTS PAGE NO.*, 97.
- [33]. Khan, F., & Nakagawa, K. (2012). B-8-10 Cooperative Spectrum Sensing Techniques in Cognitive Radio Networks. *電子情報通信学会ソサイエティ大会講演論文集*, 2012(2), 152.
- [34]. Safdar, M., Khan, I. A., Ullah, F., Khan, F., & Jan, S. R. Comparative Study of Routing Protocols in Mobile Adhoc Networks.
- [35]. Shahzad Khan, Fazlullah Khan, Fahim Arif, Qamar Jabeen, M.A Jan and S. A Khan (2016). "Performance Improvement in Wireless Sensor and Actor Networks", *Journal of Applied Environmental and Biological Sciences*, Vol. 6(4S), pp. 191-200, Print ISSN: 2090-4274 Online ISSN: 2090-4215, TextRoad.
- [36]. M. Usman, M. A. Jan, X. He and P. Nanda, "Data Sharing in Secure Multimedia Wireless Sensor Networks," in *15th IEEE International Conference on Trust, Security and Privacy in Computing and Communications (IEEE TrustCom-16)*, "accepted", 2016.