International Journal of Computer Applications Technology and Research
Volume 5 issue 7, 500 – 503, 2016, ISSN: - 2319-8656

Comparative Study of RISC AND CISC Architectures

Shahzeb[1], Naveed Hussain[1], Amanulllah[1], Furqan Ahmad[1], Salman Khan[1]
[1]Department of Computer Science, Abdul Wali Khan University Mardan, KPK, Pakistan

Abstract- Comparison between RISC and CISC in the language of computer architecture for research is not very simple because a lot of researcher worked on RISC and CISC Architectures. Both these architecture differ substantially in terms of their underlying platforms and hardware architectures. The type of chips used differs a lot and there exists too many variants as well. This paper gives us the architectural comparison between RISC and CISC architectures. Also, we provide their advantages performance point of view and share our idea to the new researchers.

Keywords: RISC, CISC, Architecture, AMD

I. INTRODUCTION

The Microprocessor chips are divided into two categories. In both of these architectures the main purpose is to optimal the performance of the system. Our Research on these two architecture which is complex but we do our best [1-8]. CISC is stand for complex instruction set computer. Nowadays the PCs mostly uses CISC architecture Like AMD and Intel etc. CISC chips have large and complex instructions [9-13]. We know that hardware is faster than software so therefore one should make a powerful instruction set which provides programmers with assembly instructions to do a lot with short program. In common CISC chips are relatively slow (as compared to RISC).

RISC is stand for Reduced Instruction Set Computer. Nowadays mostly Mobile Phones Based on RISC architecture Like MIPS and ARM etc. RISC has simple and small Instruction. RISC chips Comes around the mid 80's because the reaction of CISC chips. The philosophy behind that almost no one use complex instructions and mostly people uses compilers which never use complex instructions. So for Apple uses RISC chips [14-20]. So therefore simple and faster instructions are better than large complex and slower (CISC) instructions. However, RISC required more instruction to complete a task than CISC. An advantage of RISC is that because it more simple instructions. RISC chips require less transistors which makes easier to design and cheaper to produce. So now it easier to write powerful optimal compilers since fewer instructions exists.

II. COMPARISON OF RISC AND CISC

First we explain the properties of CISC architectures and then we explain the properties of RISC architecture.

Properties of CISC:

1. Some simple and very complex instructions
2. In CISC instructions take more than 1 clock per Cycle to execute
3. Variable size instructions
4. No pipelining
5. Few registers
6. Not a load and store machine
7. For Compilation not so good in term of speed
8. Emphasis of Hardware
9. Transistors are used for storing complex instructions

Properties of RISC:

1. Small and simple instructions
2. In RISC Instructions are execute in one clock cycle per Instructions
3. All instructions have the same length
4. Load and Store architecture implemented due to the desired single-cycle operation
5. Have Pipelining
6. More register than CISC
7. Optimal compilation speed as compared to CISC
8. Emphasis on software
9. Compare to CISC a RISC Spends more transistors on memory registers

Examples of CISC and RISC Processors are shown in Table 1.

Table 1: RISC and CISC Architecture

CISC	RISC
IBM 370-169	MIPS R2000
VAX 11-780	SUN SPARC
MICROVAX 2	INTEL i860
INTEL 80386	MOTOROLA 8800
INTEL 80286	POWERPC 601

A. ADVANTAGES OF RISC:

Implementation with simple instructions provides many advantages over implementing as compared to CISC Processors. Simple instruction set allow for pipeline superscalar designing RISC processor often achieved two to four times performance of CISC processors using [21-27] comparable semiconductor technology and similar clock rates.

Simple hardware. Because instructions set of a (RISC) processor is so simple, it uses up much less chips spaces and extra functions i.e. memory management unit or floating point arithmetic units, can also be placed on the similar chip. Smaller chips allows a semiconductor manufacturers to placed more parts on single silicon wafer which can lower per chips cost dramatically and have short design cycles. Since RISC processors are simpler than corresponding CISC processors they can be design more quickly and take advantage of other technological [28-33] developments sooner than corresponds CISC design leading to great leaps in performance between generations.

B. Advantages of CISC:

At the time of their initial development CISC machines use technologies to optimize the performance of a computer. Microprogramming is easy as assembly Programming language to implement and less expensive than hardwiring a control unit.

The ease of micro coding newly instructions allows designers to make (CISC) machines upwardly compatible new computer run the same programs as early computers because the new computers would contained a superset of instructions of earlier computers. As each instruction became more capable less instruction used to implement the given task. This made efficient uses of the relative slow main memory.

Because micro program instructions set can be write to match the construct of high level languages the compilers doesn't have to be as complicated.

III. PROBLEM STATEMENT

We discussed the RISC and CISC Architectures. Nowadays the Technology is growing rapidly the problem is that how fix the problem of performance between Risc and Cisc to overcome the Comments of different architecture [34-36] who claim the issues of Performance.

IV. PROPOSED IDEA

We study a lot of Research Articles Our statistics is 40 to 50 percent Researchers talk about the same issues. So in our idea is to combine these to Architectures and make a hybrid processor to overcome the problem but it is not so simple it take a lot of time. We call Fresher Students or Professionals to do work on the hybrid processor based on Risc and Cisc which will be helps the designers and developers.

The motivation for the design of RISC processors arose from technological developments which changed gradually the architectural parameters traditionally used in the computer industry. Researchers have already given a detailed account of the prehistory of RISC. At the abstract architectural level the general trend until the middle of the seventies was the design of ever richer instruction sets which could take some of the burden of interpreting high level computer languages from the compiler to the hardware. The philosophy of the time was to build machines which could diminish the semantic gap between high level languages and the machine language. Many special instructions were included in the instruction set in order to improve the performance of some operations and several machine instructions looked almost like their high-level counterparts. If anything was to be avoided it was, first of all, compiler complexity. At the implementation level, microcoding provided a general method of implementing increasingly complex instruction sets using a fair amount of hardware. Microcoding also made possible to develop families of compatible computers which differed only in the underlying technology and performance level, like in the case of the IBM/360 system.

The metrics used to assess the quality of a design corresponded directly to these two architectural levels: the first metric was code density, i.e., the length of compiled programs; the second metric was compiler complexity. Code density should be maximized, compiler complexity should be minimized. Not very long ago Wirth [1986] was still analyzing some microprocessor architectures based exactly

on these criteria and denouncing them for being "halfheartedly high-level language oriented."

V. CONCLUSION

In this paper we briefly explain RISC and CISC architectures on the bases of their properties and also explain their advantages. Now Due to this exploration both architectures RISC and CISC have continuously developed. The RISC architecture had advantages that the results to a machines excellent performance and adopted for commercial products. We also talk little bit about the performance problem provide idea for Researchers to further explain the Risc and Cisc and also to Clarify the new Processor based on Risc and Cisc.

REFERENCES

[1]. Khan, F., Bashir, F., & Nakagawa, K. (2012). Dual Head Clustering Scheme in Wireless Sensor Networks. in the IEEE International Conference on Emerging Technologies (pp. 1-8). Islamabad: IEEE Islamabad.

[2]. M. A. Jan, P. Nanda, X. He, Z. Tan and R. P. Liu, "A robust authentication scheme for observing resources in the internet of things environment" in 13th International Conference on Trust, Security and Privacy in Computing and Communications (TrustCom), pp. 205-211, 2014, IEEE.

[3]. Khan, F., & Nakagawa, K. (2012). Performance Improvement in Cognitive Radio Sensor Networks. in the Institute of Electronics, Information and Communication Engineers (IEICE) , 8.

[4]. M. A. Jan, P. Nanda and X. He, "Energy Evaluation Model for an Improved Centralized Clustering Hierarchical Algorithm in WSN," in Wired/Wireless Internet Communication, Lecture Notes in Computer Science, pp. 154–167, Springer, Berlin, Germany, 2013.

[5]. Khan, F., Kamal, S. A., & Arif, F. (2013). Fairness Improvement in long-chain Multi-hop Wireless Adhoc Networks. International Conference on Connected Vehicles & Expo (pp. 1-8). Las Vegas: IEEE Las Vegas, USA.

[6]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "Enhancing lifetime and quality of data in cluster-based hierarchical routing protocol for wireless sensor network", 2013 IEEE International Conference on High Performance Computing and Communications & 2013 IEEE International Conference on Embedded and Ubiquitous Computing (HPCC & EUC), pp. 1400-1407, 2013.

[7]. Q. Jabeen, F. Khan, S. Khan and M.A Jan. (2016). Performance Improvement in Multihop Wireless Mobile Adhoc Networks. *in the Journal Applied, Environmental, and Biological Sciences (JAEBS*), vol. 6(4S), pp. 82-92. Print ISSN: 2090-4274 Online ISSN: 2090-4215, TextRoad.

[8]. Khan, F., & Nakagawa, K. (2013). Comparative Study of Spectrum Sensing Techniques in Cognitive Radio Networks. in IEEE World Congress on Communication and Information Technologies (p. 8). Tunisia: IEEE Tunisia.

[9]. Khan, F. (2014). Secure Communication and Routing Architecture in Wireless Sensor Networks. the 3rd Global Conference on Consumer Electronics (GCCE) (p. 4). Tokyo, Japan: IEEE Tokyo.

[10]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "PASCCC: Priority-based application-specific congestion control clustering protocol" Computer Networks, Vol. 74, PP-92-102, 2014.

[11]. Khan, F. (2014, May). Fairness and throughput improvement in multihop wireless ad hoc networks. In *Electrical and Computer Engineering (CCECE), 2014 IEEE 27th Canadian Conference on* (pp. 1-6). IEEE.

[12]. Mian Ahmad Jan and Muhammad Khan, "A Survey of Cluster-based Hierarchical Routing Protocols", in IRACST–International Journal of Computer Networks and Wireless Communications (IJCNWC), Vol.3, April. 2013, pp.138-143.

[13]. Khan, S., Khan, F., & Khan, S.A.(2015). Delay and Throughput Improvement in Wireless Sensor and Actor Networks. 5th National Symposium on Information Technology: Towards New Smart World (NSITNSW) (pp. 1-8). Riyadh: IEEE Riyad Chapter.

[14]. Khan, F., Khan, S., & Khan, S. A. (2015, October). Performance improvement in wireless sensor and actor networks based on actor repositioning. In *2015 International Conference on Connected Vehicles and Expo (ICCVE)* (pp. 134-139). IEEE.

[15]. Khan, S., Khan, F., Jabeen. Q., Arif. F., & Jan. M. A. (2016). Performance Improvement in Wireless Sensor and Actor Networks. in the Journal Applied, Environmental, and Biological Sciences Print ISSN: 2090-4274 Online ISSN: 2090-4215

[16]. Mian Ahmad Jan and Muhammad Khan, "Denial of Service Attacks and Their Countermeasures in WSN", in IRACST–International Journal of Computer Networks and Wireless Communications (IJCNWC), Vol.3, April. 2013.

[17]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "A Sybil Attack Detection Scheme for a Centralized Clustering-based Hierarchical Network" in Trustcom/BigDataSE/ISPA, Vol.1, PP-318-325, 2015, IEEE.

[18]. Jabeen, Q., Khan, F., Hayat, M.N., Khan, H., Jan., S.R., Ullah, F., (2016) A Survey : Embedded Systems Supporting By Different Operating Systems in the International Journal of Scientific Research in Science, Engineering and Technology(IJSRSET), Print ISSN : 2395-1990, Online ISSN : 2394-4099, Volume 2 Issue 2, pp.664-673.

[19]. Syed Roohullah Jan, Syed Tauhid Ullah Shah, Zia Ullah Johar, Yasin Shah, Khan, F., " An Innovative Approach to Investigate Various Software Testing Techniques and Strategies", International Journal of Scientific Research in Science, Engineering and Technology(IJSRSET), Print ISSN : 2395-1990, Online ISSN : 2394-4099, Volume 2 Issue 2, pp.682-689, March-April 2016. URL : http://ijsrset.com/IJSRSET1622210.php

[20]. Khan, F., Jan, SR, Tahir, M., & Khan, S., (2015) Applications, Limitations, and Improvements in Visible Light Communication Systems" In *2015 International Conference on Connected Vehicles and Expo (ICCVE)* (pp. 259-262). IEEE.

[21]. Syed Roohullah Jan, Khan, F., Muhammad Tahir, Shahzad Khan,, (2016) "Survey: Dealing Non-Functional Requirements At Architecture Level", VFAST Transactions on Software Engineering, (Accepted 2016)

[22]. M. A. Jan, "Energy-efficient routing and secure communication in wireless sensor networks," Ph.D. dissertation, 2016.

[23]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Lightweight Mutual Authentication Scheme for IoT Objects," *IEEE Transactions on Dependable and Secure Computing (TDSC)*, "Submitted", 2016.

[24]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Sybil Attack Detection Scheme for a Forest Wildfire Monitoring Application," *Elsevier Future Generation Computer Systems (FGCS)*, "Accepted", 2016.

[25]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2015, August). DPBSV--An Efficient and Secure Scheme for Big Sensing Data Stream. InTrustcom/BigDataSE/ISPA, 2015 IEEE (Vol. 1, pp. 246-253). IEEE.

[26]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2015). A Dynamic Key Length Based Approach for Real-Time Security Verification of Big Sensing Data Stream. In Web Information Systems Engineering–WISE 2015 (pp. 93-108). Springer International Publishing.

[27]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2016). A dynamic prime number based efficient security mechanism for big sensing data streams.Journal of Computer and System Sciences.

[28]. Puthal, D., & Sahoo, B. (2012). Secure Data Collection & Critical Data Transmission in Mobile Sink WSN: Secure and Energy efficient data collection technique.

[29]. Puthal, D., Sahoo, B., & Sahoo, B. P. S. (2012). Effective Machine to Machine Communications in Smart Grid Networks. ARPN J. Syst. Softw.© 2009-2011 AJSS Journal, 2(1), 18-22.

[30]. M. A. Jan, P. Nanda, M. Usman, and X. He, "PAWN: A Payload-based mutual Authentication scheme for Wireless Sensor Networks*,"* "accepted", 2016.

[31]. M. Usman, M. A. Jan, and X. He, "Cryptography-based Secure Data Storage and Sharing Using HEVC and Public Clouds," *Elsevier Information sciences*, "accepted", 2016.

[32]. Jan, S. R., Khan, F., & Zaman, A. THE PERCEPTION OF STUDENTS ABOUT MOBILE LEARNING AT UNIVERSITY LEVEL. *NO. CONTENTS PAGE NO.*, 97.

[33]. Khan, F., & Nakagawa, K. (2012). B-8-10 Cooperative Spectrum Sensing Techniques in Cognitive Radio Networks. 電子情報通信学会ソサイエティ大会講演論文集, *2012*(2), 152.

[34]. Safdar, M., Khan, I. A., Ullah, F., Khan, F., & Jan, S. R. Comparative Study of Routing Protocols in Mobile Adhoc Networks.

[35]. Shahzad Khan, Fazlullah Khan, Fahim Arif, Qamar Jabeen, M.A Jan and S. A Khan (2016). "Performance Improvement in Wireless Sensor and Actor Networks", Journal of Applied Environmental and Biological Sciences, Vol. 6(4S), pp. 191-200, Print ISSN: 2090-4274 Online ISSN: 2090-4215, TextRoad.

[36]. M. Usman, M. A. Jan, X. He and P. Nanda, "Data Sharing in Secure Multimedia Wireless Sensor Networks," *in 15th IEEE International Conference on Trust, Security and Privacy in Computing and Communications (IEEE TrustCom-16)*, "accepted", 2016.